STIC Search Report
EIC 2800

STIC Database Tracking Number: 127867

TO: Monica Lewis **Location: JEF 5A30** **Art Unit : 2822** **Tuesday, July 27, 2004** **Case Serial Number: 09/849537**	**From: Irina Speckhard** **Location: EIC 2800 JEF 4B59** **Phone: (571) 272-2554** **irina.speckhard@uspto.gov**

Search Notes

Examiner Lewis,

Please find attached prior-art search results from the patent and non-patent abstract and full-text databases. The results were based on claims and statements of technical problems and solutions. Tagged records might be worth your review as well as the rest of the references provided.

If you need further searching or have questions or comments, please let me know.

Thank you,

Irina Speckhard

STIC Search Results Feedback Form

EIC 2800

Questions about the scope or the results of the search? Contact *the EIC searcher or contact*:

Jeff Harrison, EIC 2800 Team Leader
571-272-2511, JEF 4B68

Voluntary Results Feedback Form

- *I am an examiner in Workgroup:* ☐ *Example: 2810*
- *Relevant prior art **found**, search results used as follows:*
  - ☐ 102 rejection
  - ☐ 103 rejection
  - ☐ Cited as being of interest.
  - ☐ Helped examiner better understand the invention.
  - ☐ Helped examiner better understand the state of the art in their technology.

Types of relevant prior art found:

- ☐ Foreign Patent(s)
- ☐ Non-Patent Literature
  (journal articles, conference proceedings, new product announcements etc.)

- *Relevant prior art **not found:***
  - ☐ Results verified the lack of relevant prior art (helped determine patentability).
  - ☐ Results were not useful in determining patentability or understanding the invention.

Comments:

Drop off or send completed forms to STIC/EIC2800, CP4-9C13

12786?

SEARCH REQUEST FORM Scientific and Technical Information Center - EIC2800

Rev. 3/15/2004 This is an experimental format -- Please give suggestions or comments to Jeff Harrison, JEF-4B68, 272-2511.

Date 7/22/04 Serial # 09/849,537 Priority Application Date _____

Your Name M. Lewis Examiner # _____

AU 2822 Phone 272-1838 Room 5A30

In what format would you like your results? Paper is the default. (PAPER) DISK EMAIL

If submitting more than one search, please prioritize in order of need. 3 4/4

Need before 8/5

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

Where have you searched so far on this case?

Circle: USPT DWPI EPO Abs JPO Abs IBM TDB

Other: _____

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements. _____

What types of references would you like? Please checkmark:

Primary Refs ✓ Nonpatent Literature ___ Other _____

Secondary Refs ✓ Foreign Patents ___

Teaching Refs ___

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 13, 16, 17 & 52-59

Problem: See paragraphs 2-10

Solution: " " 11-16

Staff Use Only

Searcher: Jeff Harrison

Searcher Phone: _____

Searcher Location: STIC-EIC2800, JEF-4B68

Date Searcher Picked Up: 7/26/04

Date Completed: 7/26/04

Searcher Prep/Rev Time: 165

Online Time: 170

Type of Search

Structure (#)_____

Bibliographic ✓

Litigation_____

Fulltext_____

Patent Family ✓

Other AU

Vendors

STN ✓

Dialog ✓

Questel/Orbit_____

Lexis-Nexis_____

WWW/Internet_____

Other_____

```
SYSTEM:OS  - DIALOG OneSearch
  File   2:INSPEC 1969-2004/Jul W3
         (c) 2004 Institution of Electrical Engineers
*File   2: Alert feature enhanced for multiple files, duplicates
removal, customized scheduling. See HELP ALERT.
  File   6:NTIS 1964-2004/Jul W4
         (c) 2004 NTIS, Intl Cpyrght All Rights Res
  File   8:Ei Compendex(R) 1970-2004/Jul W3
         (c) 2004 Elsevier Eng.  Info. Inc.
  File  34:SciSearch(R) Cited Ref Sci 1990-2004/Jul W3
         (c) 2004 Inst for Sci Info
  File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
  File  35:Dissertation Abs Online 1861-2004/May
         (c) 2004 ProQuest Info&Learning
  File  65:Inside Conferences 1993-2004/Jul W4
         (c) 2004 BLDSC all rts. reserv.
  File  94:JICST-EPlus 1985-2004/Jul W1
         (c)2004 Japan Science and Tech Corp(JST)
  File  99:Wilson Appl. Sci & Tech Abs 1983-2004/Jun
         (c) 2004 The HW Wilson Co.
  File 144:Pascal 1973-2004/Jul W3
         (c) 2004 INIST/CNRS
  File 305:Analytical Abstracts 1980-2004/Jul W3
         (c) 2004 Royal Soc Chemistry
*File 305: Alert feature enhanced for multiple files, duplicate
removal, customized scheduling.  See HELP ALERT.
  File 315:ChemEng & Biotec Abs 1970-2004/Jun
         (c) 2004 DECHEMA
  File 350:Derwent WPIX 1963-2004/UD,UM &UP=200447
         (c) 2004  Thomson Derwent
*File 350: For more current information, include File 331 in your search.
Enter HELP NEWS 331 for details.
  File 347:JAPIO Nov 1976-2004/Mar(Updated 040708)
         (c) 2004 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed.
Alerts have been run.  See HELP NEWS 347 for details.
  File 344:Chinese Patents Abs Aug 1985-2004/May
         (c) 2004 European Patent Office
  File 371:French Patents 1961-2002/BOPI 200209
         (c) 2002 INPI.  All rts. reserv.
*File 371: This file is not currently updating. The last update is 200209.
```

Set	Items	Description
S1	17267	BALL()GRID()ARRAY OR BGA
S2	397964	SOLDER(W)BOND? OR SOLDER OR SOLDERING OR SOLDERED OR BRAZ?
S3	34529	(SOLDER?)(W)(BALL? ? OR BUMP? ? OR POST? ? OR SPHERE? OR PAD OR PADS OR PLATE?) OR BGA OR BALLGRID? ? OR BALL(W)GRID? ? OR POLYMER(W)BALL? ?
S4	408007	S1:S3
S5	16480	CONTACT?(3N)(PADS OR PAD)
S6	32203	(ELECTRICAL? OR THERMAL?)(3N)(ENHANC? OR BETTER)
S7	211486	(HEAT? OR WARM? OR HOT? OR CALEFACT? OR TORREFACT? OR PYROL? OR SINTER? OR CALCIN? OR AUTOCLAV?)(3N)(CONDUCT? OR SPREAD?)
S8	231512	(THERMOL? OR THERMAL? OR PREHEAT? OR MELT? OR FUSE? OR FUSING? ? OR FUSION?)(3N)CONDUCT?
S9	1793309	(HIGH??? OR HEIGHTEN? OR RAIS? OR INCREAS? OR ELEVAT?)(3N)(TEMPERATUR? OR CELSIUS OR DEGREE? ?)
S10	2164406	S6:S9
S11	573206	(EPOX??? OR RESIN? ? OR THERMOPLASTIC??? OR THERMO()PLASTIC???? OR ELASTOMER?? OR RUBBER? ? OR ADHESIVE??)(3N)(LAYER??? OR FILM??? OR COAT???)
S12	3660644	(POLYMER???? OR HOMOPOLYMER????? OR COPOLYMER?????)
S13	27073	MC=U11-E02A1 OR IC=H01L-021/56
S14	8252149	ADHESIVE? ? OR ADHERE??? OR ATTACH??????? OR SECUR??????? OR CONNECT???????? OR STICK???????? OR SEAL????????
S15	11534499	S11:S14
S16	2674444	AL OR ALUMINUM
S17	1516406	CU OR COPPER
S18	5	(DIE()UP)(3N)(TAPE? OR PLASTIC?)
S19	2353759	DIE OR DIED OR DIEING OR DIES OR DICE OR CUT OR CHOP OR ETCH???????? OR CUT OR TRIM?
S20	2353759	S18:S19
S21	330486	(PRINT??????(3N)CIRCUIT???????) OR (CIRCUIT????????(3N)BOARD???) OR PCB
S22	1428294	(INTEGRAT????????(3N)(CIRCUIT???????? OR LOOP? ?)) OR IC OR CHIP? ?
S23	3807617	MICRO()(ELECTRONIC? OR CIRCUIT? ? OR CHIP? ?) OR CHIP? ? OR MICROCIRCUIT? ? OR DIE? ? OR LOGIC(W)CIRCUIT? ? OR WAFER? ? OR MICROELECTRONIC OR DICE OR ELECTROD?
S24	4486600	S22:S23
S25	53848	(BOND???????? OR JOIN????????)(3N)WIRE????????
S26	7533	(BONDWIRD???????? OR WIREBOND???????? OR (WIRING OR WIRE??-??)(N)BOND???)(3N)(CHIP? ? OR LEAD? ? OR FRAME? ?)
S27	54032	S25:S26
S28	1855	S4 AND S5
S29	175	S28 AND S10
S30	136	S29 AND S15
S31	17	S30 AND S16
S32	17	RD (unique items)
S33	119	S30 NOT S31
S34	30	S33 AND S17
S35	9	S34 AND S20
S36	9	RD (unique items)
S37	21	S34 NOT S35
S38	0	S37 AND S20
S39	4	S37 AND S21

S40	4	RD (unique items)
S41	17	S37 NOT S39
S42	13	S41 AND S24
S43	12	RD (unique items)
S44	1	S43 AND S27
S45	11	S43 NOT S44
S46	11	RD (unique items)
S47	4	S41 NOT S42
S48	4	RD (unique items)
S49	89	S33 NOT S34
S50	89	S49 AND S15
S51	61	S50 AND S24
S52	12	S51 AND S27
S53	12	RD (unique items)

32/3,AB/1 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05504890
E.I. No: EIP00035088038
Title: Flip chip technology with blind-hole-clips-bump **attachment**
Author: Videkov, Valentin; Tzanova, Slavka; Philippov, Philipp
Corporate Source: Technical Univ of Sofia, Sofia, Bulg
Conference Title: Proceedings of the 1999 International Symposium on Microelectronics
Conference Location: Chicago, IL, USA Conference Date: 19991026-19991028
E.I. Conference No.: 56143
Source: Proceedings of SPIE - The International Society for Optical Engineering v 3906 1999. p 480-483
Publication Year: 1999
CODEN: PSISDG ISSN: 0277-786X
Language: English
Abstract: In this paper, we describe an alternative assembling technique for flip chip mounting without heating processes and discuss the method's advantages and limitations. The proposed construction is an **Al** substrate with blind-holes and clips chip **attachment**. Bumps on the die are made by electro-chemical deposition, in combination with a litographically applied mask. The electrical contact is obtained through a kind of clips - the microchemically thickened **contact pads** on the **Al** substrate. The blind holes for the die bumps in the **Al** substrate are made by etching. In cases of high requirements of shock-hardiness the glob-top plastic should be coated over the die on the substrate. Limitations of this method might be the level of electrical and thermal resistance of the contact, which we are studying now. If these conditions are adjusted properly, it is possible to solve the die testing, repairing and **high temperature** chip-bonding problems in MCM. (Author abstract) 10 Refs.

32/3,AB/2 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

016043649
WPI Acc No: 2004-201500/200419
XRAM Acc No: C04-079639
XRPX Acc No: N04-160057
High power **ball grid array** includes an insulating layer of high **thermal conductivity** between a semiconductor chip and **heat spreader**
Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU); SAMSUNG ELECTRONICS CO (SMSU)
Inventor: CHO T J; KIM M H; KWON H G; CHO T; KIM M; KWON H
Number of Countries: 003 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20040012928	A1	20040122	US 2003459400	A	20030610	200419	B
JP 2004023103	A	20040122	JP 2003167601	A	20030612	200419	
KR 2003096461	A	20031231	KR 200232972	A	20020612	200426	

Priority Applications (No Type Date): KR 200232972 A 20020612
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes

US 20040012928 A1 10 H05K-007/20
JP 2004023103 A 12 H01L-023/12
KR 2003096461 A H01L-023/36

Abstract (Basic): US 20040012928 A1
Abstract (Basic):

NOVELTY - High power **ball grid array** includes an insulating layer of high **thermal conductivity** between a semiconductor chip and **heat spreader.**

DETAILED DESCRIPTION - A high power **ball grid array** comprises:

(a) a printed circuit board having a through hole;

(b) **connection** pads on a bottom surface of the printed circuit board proximate the through hole;

(c) **solder balls** (210) on the bottom surface of the printed circuit board proximate the through hole and the **connection** pads;

(d) **heat spreader** on a top surface of the printed circuit board and over the through hole, where the **heat spreader** includes an insulating layer of a high **thermal conductivity;**

(e) semiconductor chip (101) mounted on the bottom surface of the **heat spreader** inside the through hole, where the semiconductor chip includes **contact pads** (201), each **contact pad** electrically **connected** to a corresponding **connection** pad; and

(f) passive film (230) filling the through hole and surrounding the semiconductor chip.

INDEPENDENT CLAIMS are also included for the following:

(a) a method for manufacturing a **heat spreader** comprising: forming first and second metal layers on first and second surfaces of an insulating layer (111); forming a region configured to **attach** to a semiconductor chip by patterning the first metal layer; cutting a first groove through the first metal layer to a first predetermined depth of the insulating layer; cutting a second groove through the second metal layer to a second predetermined depth of the insulating layer, where the first and second grooves are aligned; and forming a protection layer (115) on the first and second metal layers; and

(b) a **heat spreader** comprising: a **heat**-emitting board that is formed by sequentially depositing a supporting ceramic layer having a board shape, a heat-emitting metal layer, and a protection layer; and a lower metal layer (120) formed on a bottom surface of the supporting ceramic layer.

USE - Used as high power **ball grid array.**

ADVANTAGE - By interposing a ceramic insulating layer between semiconductor chip and **heat spreader,** charge generation between semiconductor chip and **heat spreader** is reduced, and defects such as electrostatic discharge is reduced during testing and mounting of the package.

DESCRIPTION OF DRAWING(S) - The figure is a sectional view of a high-power **BGA** package.

Semiconductor chip (101)
Heat spreader (110)
Insulating layer (111)
Protection layer (115)
Lower metal layer (120)
Black oxide layer (140)
Printed circuit board (200)
Contact pads (201)

Dam (203)
Solder balls (210)
Passive film (230)
pp; 10 DwgNo 1/12

32/3,AB/3 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

016032451
WPI Acc No: 2004-190302/200418
Related WPI Acc No: 2003-300775
XRAM Acc No: C04-075028
XRPX Acc No: N04-150993
Interconnect module for supporting integrated circuit chip, has chip **attach** surface defining **contact pads**, board **attach** surface and conductive paths that interconnect first **contact pads** to first conductive layer
Patent Assignee: 3M INNOVATIVE PROPERTIES CO (MINN); HANSON D A (HANS-I); PETEFISH W G (PETE-I); SYLVESTER M F (SYLV-I)
Inventor: HANSON D A; PETEFISH W G; SYLVESTER M F
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20040012938	A1	20040122	US 2002199926	A	20020719	200418	B
TW 559955	A	20031101	TW 2002119135	A	20020823	200425	

Priority Applications (No Type Date): US 2002199926 A 20020719; US 2001314905 P 20010824
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20040012938	A1		21	H05K-007/02	
TW 559955	A			H01L-021/322	

Abstract (Basic): US 20040012938 A1
Abstract (Basic):
NOVELTY - An interconnect module (12) comprises a chip (14) **attach** surface defining first **contact pads** for **attachment** to integrated circuit chip; board **attach** surface defining second **contact pads** for **attachment** to printed wiring board (16); capacitor structure having first conductive layer, second conductive layer, and first dielectric layer; and conductive paths, formed in interconnect module, that interconnect first **contact pads** to the first conductive layer.
DETAILED DESCRIPTION - An interconnect module comprises:
(a) a chip **attach** surface defining first **contact pads** for **attachment** to an integrated circuit chip;
(b) a board **attach** surface defining second **contact pads** for **attachment** to a printed wiring board;
(c) a capacitor structure having a first conductive layer, a second conductive layer, and a first dielectric layer formed between the first and second conductive layers, where the first conductive layer, the second conductive layer, and the first dielectric layer are laminated together; and
(d) conductive paths, formed in the interconnect module, that interconnect first **contact pads** to the first conductive layer.
The first **contact pads**, the conductive paths, and the capacitor structure produce a combined impedance of at most0.60 ohms at

a frequency of at least1.0 GHz. An INDEPENDENT CLAIM is also included for formation of an interconnect module, comprising:

(a) providing a laminated capacitor structure having a first conductive layer, a second conductive layer, and a dielectric layer formed between the first and second conductive layers and laminated into a unitary structure;

(b) forming a chip **attach** surface defining first **contact pads** for **attachment** of an integrated circuit chip to the interconnect module on a first side of the capacitor structure;

(c) forming a board **attach** surface defining second **contact pads** for **attachment** of the interconnect module to a printed wiring board on a second side of the capacitor structure; coupling the capacitor structure, the chip **attach** surface, and the board **attach** surface to form the interconnect module; and

(d) forming conductive paths that interconnect the first **contact pads** to the first conductive layer.

USE - For use in semiconductor industry to mechanically support integrated circuit chip and electrically **attach** the chips to printed wiring boards.

ADVANTAGE - The interconnect module is provides reduced power distribution impedance an, and thus promote higher frequency operation. It is capable of reliably **attaching** an integrated circuit chip to a printed wiring board via **solder ball connections**, while providing reduced power distribution impedance of at most 0.60 ohms at operating frequencies in excess of 1 GHz.

DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional view of an electronic package incorporating an interconnect module.

Electronic package (10)
Interconnect module (12)
Chip (14)
Printed wiring board (16)
Solder ball connections (18)
pp; 21 DwgNo 1/7

32/3,AB/4 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

016008571
WPI Acc No: 2004-166422/200416
Related WPI Acc No: 2004-155095
XRAM Acc No: C04-065962
XRPX Acc No: N04-132566
Integrated circuit chip for semiconductor device, comprises metal network of electrical power distribution lines, electrical conductors, and additional electrically non-functional conductors
Patent Assignee: TEXAS INSTR INC (TEXI)
Inventor: EFLAND T R
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6597065	B1	20030722	US 2000246081	P	20001103	200416	B
			US 20012022	A	20011031		

Priority Applications (No Type Date): US 2000246081 P 20001103; US 20012022 A 20011031
Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes
US 6597065 B1 9 H01L-023/34 Provisional application US 2000246081

Abstract (Basic): US 6597065 B1
Abstract (Basic):

NOVELTY - Integrated circuit chip for semiconductor device, comprises metal network of electrical power distribution lines, electrical conductors, and additional electrically non-functional conductors.

DETAILED DESCRIPTION - An integrated circuit chip comprises active components on its active surface; a metal network of electrical power distribution lines deposited on chip surface directly over the active components, and electrically and thermally **connected** vertically to selected active components; electrical conductors for **connecting** the distribution lines to an outside source; and additional electrically non-functional conductors distributed on the lines for steepening the temperature gradient for thermal flux away from the active components and lines. The power distribution lines have a **thermal conductance** at least an order of magnitude greater than underlying thin film electrical interconnects.

An INDEPENDENT CLAIM is also included for a semiconductor device a semiconductor chip having first and second surfaces; an integrated circuit fabricated on first chip surface, and protected by a mechanically strong, electrically insulating overcoat having metal-filled vias to contact at least one metal layer; conductive films deposited on the overcoat and patterned into a network of lines vertically over the active components; electrical conductors **connecting** the network lines to an outside electrical source; and additional **thermal**-only **conductors** distributed on the lines for thermal flux away from the lines to an outside heat sink. The films are in contact with the vias, and have at least one stress-absorbing film and a non-corrodible and metallurgically **attachable** outermost film. The network is patterned to spread thermal energy and distribute electrical power current and ground potential.

USE - For semiconductor device.

ADVANTAGE - The network provides effective **heat-spreader** directly over and close by the heat-generating integrated circuit (IC) components. It relocates most of the conventional power distribution interconnections from the critical circuit level to newly created surface network, thus saving silicon real state and permitting shrinkage of the IC area.

DESCRIPTION OF DRAWING(S) - The figure is a simplified and schematic perspective view of integrated circuit chip.

Solder balls (301, 302, 311, 312)

Bonding wires (371, 372, 381, 382)

pp; 9 DwgNo 3/3

32/3,AB/5 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015948882
WPI Acc No: 2004-106723/200411
XRAM Acc No: C04-043434
XRPX Acc No: N04-084808
Wire-bonded chip on board package has substrate made of material including first resin, **solder** mask made of material including second resin, integrated circuit chip, wire bonds and molding material
Patent Assignee: ULTRATERA CORP (ULTR-N); CHIH W (CHIH-I); MAA C (MAAC-I);

SHAN W (SHAN-I); TSAI M (TSAI-I)
Inventor: CHIH W; MAA C; SHAN W; TSAI M; CHR W; DAN W; MA C
Number of Countries: 029 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030205793	A1	20031106	US 2002152770	A	20020523	200411	B
EP 1365450	A1	20031126	EP 2002253673	A	20020524	200411	N
KR 2003086192	A	20031107	KR 200228991	A	20020524	200418	
TW 560021	A	20031101	TW 2002109192	A	20020501	200425	

Priority Applications (No Type Date): TW 2002109192 A 20020501; EP 2002253673 A 20020524
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030205793	A1		5	H01L-023/02	
EP 1365450	A1	E		H01L-023/498	
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR					
KR 2003086192	A			H01L-023/12	
TW 560021	A			H01L-023/28	

Abstract (Basic): US 20030205793 A1
Abstract (Basic):
NOVELTY - A wire-bonded chip on board package comprises:
(a) a substrate made of a material including a first resin;
(b) a **solder** mask made of a material including a second resin;
(c) an integrated circuit chip;
(d) wire bonds electrically **connecting** electrical **contact pads** of the chip to an exposing area of conductive patterns of a substrate top surface; and
(e) a molding material encapsulating the chip, the wire bonds and the substrate top surface
DETAILED DESCRIPTION - A wire-bonded chip on board package comprises:
(a) a substrate (14) having planar opposing top and bottom surfaces with conductive patterns (24, 26), and made of a material including a first resin;
(b) a **solder** mask (40) made of a material including a second resin;
(c) an integrated circuit (IC) chip having an active side (18), an inactive side (20) and electrical **contact pads** (22) on the active side;
(d) wire bonds (34) electrically **connecting** the electrical **contact pads** of the IC chip (12) to the exposing area of the conductive patterns of the substrate top surface; and
(e) a molding material (16) encapsulating the IC chip, the wire bonds and the substrate top surface. The second resin has a thermal expansion coefficient identical to that of the first resin of the substrate on the top surface of the substrate such that it has a smooth outer surface and openings. Each opening exposes a respective area of the conductive patterns of the substrate. The IC chip is mechanically mounted to an outer surface (42) of the **solder** mask with the inactive side of the chip.
USE - Wire-bonded chip on board package.
ADVANTAGE - The package has a thickness thinner than that of a conventional package. It has high mechanical reliability and improved heat dissipation characteristics. The reliability of the package will be improved. The package needs only an extremely thin **layer** of **epoxy adhesive** to mount the chip on the substrate. The

thickness and the production cost of the package will be significantly reduced. Further, because of the **thermally** and electrically **conductive** layer filled in the active (upper) side of the IC chip, the package renders more efficient heat dissipation and **better electrical** performance.

DESCRIPTION OF DRAWING(S) - The figure is a cross-section of a wire-bonded chip on board package.

IC chip (12)
Substrate (14)
Molding material (16)
Active side (18)
Inactive side (20)
Electrical **contact pads** (22)
Conductive patterns (24, 26)
Conductive vias (28)
Layer of **epoxy adhesive** (30)
Wire bonds (34)
Solder mask (40)
Outer surface (42)
pp; 5 DwgNo 1/3

32/3,AB/6 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015911379
WPI Acc No: 2004-069219/200407
XRAM Acc No: C04-028720
XRPX Acc No: N04-055655
Improved flip chip package comprises substrate member having top and bottom surfaces and conductive pattern, **solder** mask, integrated circuit chip, **solder bumps**, and molding material encapsulating chip and top surface of substrate
Patent Assignee: ULTRATERA CORP (ULTR-N); UNITED TEST CENT INC (UNTE-N); CHIH W (CHIH-I); MAA C (MAAC-I); SHAN W (SHAN-I); TSAI M (TSAI-I)
Inventor: CHIH W; MAA C; SHAN W; TSAI M; CHR W; MA C
Number of Countries: 029 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030201544	A1	20031030	US 2002152616	A	20020523	200407	B
EP 1369919	A1	20031210	EP 2002253674	A	20020524	200407	N
TW 550717	A	20030901	TW 2002108921	A	20020430	200413	
KR 2003085449	A	20031105	KR 200228990	A	20020524	200418	

Priority Applications (No Type Date): TW 2002108921 A 20020430; EP 2002253674 A 20020524
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030201544	A1		6	H01L-023/48	
EP 1369919	A1	E		H01L-023/498	
	Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR				
TW 550717	A			H01L-021/60	
KR 2003085449	A			H01L-023/28	

Abstract (Basic): US 20030201544 A1
Abstract (Basic):
NOVELTY - An improved flip chip package (40) comprises substrate member (14) having top and bottom surfaces, and conductive pattern;

solder mask made of material having second resin; integrated circuit (IC) chip (12) having active side, inactive side, and electrical **contact pads** on active side; **solder bumps** formed on respective **contact pads**; and molding material (42) encapsulating chip and top surface of the substrate.

DETAILED DESCRIPTION - Improved flip chip package comprises substrate member having top and bottom surfaces, and conductive pattern; **solder** mask made of material having second resin; integrated circuit (IC) chip having active side, inactive side, and electrical **contact pads** on active side; **solder bumps** formed on respective **contact pads**; and molding material encapsulating chip and top surface of the substrate. The substrate is made of material having first resin. The **solder** mask is disposed on the top surface of the substrate so that a smooth surface is formed. The outer surface has opening that exposes a respective area of the conductive pattern of the substrate.

USE - For use as improved flip chip package.

ADVANTAGE - The invention has low cost, superior heat dissipation characteristics, and good electrical performance. It also provides high package reliability.

DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional side view of a flip chip package.

IC chip (12)
Substrate member (14)
Improved flip chip package (40)
Molding material (42)
Thermally and electrically **conductive** layer (44)
pp; 6 DwgNo 3/4

32/3,AB/7 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015725010
WPI Acc No: 2003-787210/200374
XRAM Acc No: C03-217190
XRPX Acc No: N03-630801
Semiconductor device comprises semiconductor chip having planar active surface including integrated circuit protected with inorganic overcoat
Patent Assignee: TEXAS INSTR INC (TEXI); KODURI S K (KODU-I); ZUNIGA-ORTIZ E R (ZUNI-I)
Inventor: KODURI S K; ZUNIGA-ORTIZ E R
Number of Countries: 033 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030141593	A1	20030731	US 200257138	A	20020125	200374	B
JP 2003224158	A	20030808	JP 200317274	A	20030127	200374	
EP 1333494	A2	20030806	EP 2003100143	A	20030123	200374	

Priority Applications (No Type Date): US 200257138 A 20020125
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030141593	A1		13	H01L-023/48	
JP 2003224158	A		11	H01L-021/60	
EP 1333494	A2	E		H01L-023/485	

Designated States (Regional): AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LI LT LU LV MC MK NL PT RO SE SI SK TR

Abstract (Basic): US 20030141593 A1

Abstract (Basic):

NOVELTY - A semiconductor device (201) comprises semiconductor chip having planar active surface (201a) with integrated circuit protected with inorganic overcoat (203). The circuit has metallization patterns (202) with **contact pads** having added conductive layer (205) on metallization. The added layer has conformal surface adjacent chip, peripheral portions of overcoat, and planar outer surface for forming metallurgical bonds without melting.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for:

(a) a semiconductor assembly comprising semiconductor chip having planar active surface including integrated circuit, and assembly board having planar metallurgically bondable terminal pads in a distribution aligned with the distribution of chip **contact pads**;

(b) a method of fabricating a semiconductor device comprising depositing added conductive layer on metallization of **contact pads**; and

(c) a method for fabricating semiconductor assembly comprising providing semiconductor chip having planar active surface with integrated circuit protected by inorganic overcoat, providing assembly board having planar metallurgically bondable material pads, aligning added chip metallization and board pads, and metallurgically bonding chip metallization and board pads.

USE - For use as a semiconductor device.

ADVANTAGE - The method employs a wide variety of materials and techniques. It has reduced manufacturing cost, lead-free assembly solution, improved thermal performance of the package, and improved reliability of the device.

DESCRIPTION OF DRAWING(S) - The figure is a schematic cross section of the semiconductor device showing a **layer** of nonconductive **adhesive**.

Semiconductor device (201)
Planar active surface (201a)
Metallization patterns (202)
Inorganic overcoat (203)
Added conductive layer (205)
pp; 13 DwgNo 3/11

32/3,AB/8 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015269796
WPI Acc No: 2003-330725/200331
XRAM Acc No: C03-085804
XRPX Acc No: N03-264829
Semiconductor structure for flip chip mounting to substrate comprises silicon substrate, amorphous oxide material, perovskite oxide material, and compound semiconductor material
Patent Assignee: MOTOROLA INC (MOTI)
Inventor: BOSCO B A; EMRICK R M; ESCALERA N J; ROCKWELL S K
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030015709	A1	20030123	US 2001906138	A	20010717	200331	B

Priority Applications (No Type Date): US 2001906138 A 20010717
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030015709	A1		28	H01L-031/256	

Abstract (Basic): US 20030015709 A1
Abstract (Basic):

NOVELTY - A semiconductor structure (34) for flip chip mounting to substrate (22) has monocrystalline silicon substrate, amorphous oxide material (36) overlying the substrate, monocrystalline perovskite oxide material overlying the amorphous material, and monocrystalline compound semiconductor material overlying the perovskite oxide material.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for:

(1) a process for fabricating the semiconductor structure comprising providing the substrate, depositing the perovskite oxide film having a thickness less than that of the material that would result in strain-induced defects, forming amorphous oxide interface layer between the perovskite film and substrate, epitaxially forming the semiconductor layer, and forming an array of electrically conductive pads overlying surface of the structure; and

(2) a process for fabricating a microelectronic assembly including the semiconductor structure bonded to substrate comprising the steps of forming the semiconductor structure.

The fabrication of the assembly includes forming a passivation layer including apertures to expose an area of the pads, forming an array of **solder bumps** in contact with the array of the pads, positioning the structure in association with the substrate, and bonding the structure with the substrate.

USE - The device is used in microelectronic assembly and is configured for flip-chip mounting to substrate (claimed).

ADVANTAGE - The device does not require large numbers of input/output points. The increasing size of the packaging bodies does not limit the number and spacing of semiconductor devices that can be placed on a particular circuit board or substrate. This does not lengthen the conductive paths and interconnection lengths between semiconductor devices thus, not limiting their overall performance.

DESCRIPTION OF DRAWING(S) - The figure shows schematically, in cross-section, the device.

Substrate (22)
Semiconductor structure (34)
Amorphous layer (36)
pp; 28 DwgNo 3/33

32/3,AB/9 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014649340
WPI Acc No: 2002-470044/200250
XRAM Acc No: C02-133624
XRPX Acc No: N02-370990
Filled **solder** material for microelectronic device packaging, includes coated filler particles disposed within the **solder** material
Patent Assignee: INTEL CORP (ITLC)
Inventor: KONING P A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6365973	B1	20020402	US 99457057	A	19991207	200250	B

Priority Applications (No Type Date): US 99457057 A 19991207
Patent Details:

Patent No Kind Lan Pg   Main IPC   Filing Notes
US 6365973   B1   8 H01L-023/48

Abstract (Basic): US 6365973 B1
Abstract (Basic):
NOVELTY - A filled **solder** material comprises **solder** material (116) and coated filler particles (102) disposed within the **solder** material. The filler particles comprise first material with a coating material. The first material comprises a material different from the coating material.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a microelectronic package comprising microelectronic device (104) and **solder balls**. The microelectronic device has an active surface (112). The **solder balls** are discretely disposed on **contact pads** (114) on the microelectronic device active surface.
USE - For microelectronic device packaging.
ADVANTAGE - The inventive **solder** material includes a filler material having low CTE. The utilization of this filler material results to lower thermal mismatch and less internal stress during thermal cycling, thus providing more reliable **attachment**.
DESCRIPTION OF DRAWING(S) - A side cross-sectional view of a microelectronic device **attached** to a substrate with the inventive filled **solder balls**.
Microelectronic device (104)
Active surface (112)
Contact pads (114)
Conductive material (122)
Coating material (124)
pp; 8 DwgNo 1/4

32/3,AB/10   (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014219419
WPI Acc No: 2002-040117/200205
XRAM Acc No: C02-011386
XRPX Acc No: N02-029646
Ball grid array interconnection structure, comprises spheres joined to module by electrically conductive **adhesive** comprising thermoplastic or thermosetting resin matrix, no-clean **solder** flux and conductive particles
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: CALL A J; DELAURENTIS S A; FAROOQ S; KANG S K; PURUSHOTHAMAN S; STALTER K A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6297559	B1	20011002	US 9752175	A	19970710	200205	B
			US 98107998	A	19980630		

Priority Applications (No Type Date): US 9752175 P 19970710; US 98107998 A 19980630
Patent Details:
Patent No Kind Lan Pg   Main IPC   Filing Notes
US 6297559   B1   10 H01L-023/48   Provisional application US 9752175

Abstract (Basic): US 6297559 B1

Abstract (Basic):

NOVELTY - **Ball grid array** structure has electrically conductive spheres joined to a chip carrier module by electrically conductive **adhesive** (ECA) and printed wiring board by **solder** paste respectively. ECA contains thermoplastic/thermosetting **polymer** resin matrix, no-clean **solder** flux and electrically conductive particles (EP) having electrically conductive fusible coating. Some EP are fused through the coating.

DETAILED DESCRIPTION - Ball gid array structure comprises an array of electrically conductive spheres (34), disposed on an electronic chip carrier module (31). The spheres are electrically and mechanically joined to terminal pads on the module by an electrically conductive **adhesive** (33). The spheres are electrically and mechanically joined to printed circuit board (36) by **solder** paste (35). The conductive **adhesive** comprises thermoplastic or thermosetting **polymer** resin matrix, no-clean **solder** flux and several electrically conductive particles. The electrically conductive particles are coated by electrically conductive and fusible coating. At least some of **conductive** particles are **fused** with each other through electrically conductive fusible coating.

USE - For interconnecting micro-electronic packages and printed circuit boards.

ADVANTAGE - The structure such as **ball grid array** package (**BGA**) has longer fatigue life. The structure provides stronger and compliant interconnections of **ball grid array** package to ceramic or plastic substrates. **BGA** structure is stable and does not cause an excessive inter diffusion between **solder ball** and adjoining **solder** paste.

DESCRIPTION OF DRAWING(S) - The figures show the schematic cross-sectional representation of new **solder ball connection** scheme in ceramic **ball grid array** package.

Module (31)
Electrically conductive **adhesive** (33)
Spheres (34)
Solder paste (35)
Printed circuit board (36)
pp; 10 DwgNo 3, 5/5

32/3,AB/11 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014140143
WPI Acc No: 2001-624354/200172
XRAM Acc No: C01-186157
XRPX Acc No: N01-465156
Electrical **connection** production between conductive member and **conductor** involves application of **heat** and/or pressure to second portion of dielectric layer and conductive member(s)
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: ANDERSON S W; ARMEZZANI G J; LABZENTIS D P
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6281437	B1	20010828	US 99437506	A	19991110	200172	B

Priority Applications (No Type Date): US 99437506 A 19991110

Patent Details:
Patent No Kind Lan Pg   Main IPC   Filing Notes
US 6281437   B1   7 H01L-023/02

Abstract (Basic): US 6281437 B1
Abstract (Basic):
NOVELTY - An electrical **connection** between a conductive member and a conductor involves the application of heat and/or pressure to a second portion of a dielectric layer (17) and conductive member(s). The conductive member has a dielectric layer having a first portion with a first thickness and a second portion with a second thickness.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for the production of an electronic package as a tape **ball grid array** package including a flexible circuitized substrate (13) and an electrical component.
USE - For forming an electrical **connection** between conductive member and conductor for personal computers (PCs) or mainframe processors.
ADVANTAGE - Provides a reduced thickness that assures heat flow (and possibly displacement of the dielectric in this region, e.g. it melts back) thus facilitate bond formation, but also is able to positively retain conductors of the substrate in spaced alignment during the bonding to respective **solder balls** or chip contact sites (23).
DESCRIPTION OF DRAWING(S) - The figure is a view of an electronic package.
Flexible circuitized substrate (13)
Dielectric layer (17)
Contact sites (23)
Solder ball (33)
Contact pad (39)
pp; 7 DwgNo 1/3

32/3,AB/12   (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013823393
WPI Acc No: 2001-307605/200132
XRAM Acc No: C01-094895
XRPX Acc No: N01-220146
Electronic chip assembly includes flat, **thermally conductive** lid disposed on the chip and in thermal contact with the **thermally conductive** material, in which the lid has greater horizontal extent than the chip
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: SHERIF R; TOY H T; WOMAC D J
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No   Kind   Date   Applicat No   Kind   Date   Week
US 6222263   B1 20010424 US 99420765   A   19991019 200132 B

Priority Applications (No Type Date): US 99420765 A 19991019
Patent Details:
Patent No Kind Lan Pg   Main IPC   Filing Notes
US 6222263   B1   5 H01L-023/34

Abstract (Basic): US 6222263 B1

Abstract (Basic):

NOVELTY - An electronic chip assembly comprises a substantially flat, **thermally conductive** lid is disposed on the chip and in thermal contact with the **thermally conductive** material. The lid has a greater horizontal extent than the chip, and has an overhanging portion having at least three apertures. At least three pads are disposed on the substrate, beneath each of the three apertures respectively.

DETAILED DESCRIPTION - An electronic chip assembly in which structural support is provided, comprises a substrate (20) having a surface with electrical **connections**. An electronic chip (16) is affixed face down to the surface of the substrate, to make electrical **connections** to the **conductors**. A **thermally conductive** material (14) is disposed on the non-surface down side of the chip. A substantially flat, **thermally conductive** lid (10) is disposed on the chip and in thermal contact with the **thermally conductive** material. The lid has a greater horizontal extent than the chip. It has an overhanging portion having at least three apertures (11) which are countersunk on the side(s). At least three pads (50) are disposed on the substrate, beneath each of the three apertures respectively. A hardenable **adhesive** material (15) is disposed within the apertures and in **contact** with the **pads** and the lid, to bond the lid to the substrate.

USE - As a chip assembly.

ADVANTAGE - The invention prevents damage to circuit chip devices, and promotes the utilization of land grid array (LGA) interconnection techniques for interconnection between the module and the board.

DESCRIPTION OF DRAWING(S) - The figure shows a cross -sectional view of the aperture, **adhesive**, pad structures.

Lid (10)
Apertures (11)
Thermally conductive material (14)
Hardenable **adhesive** material (15)
Electronic chip (16)
Substrate (20)
Pads (50)
pp; 5 DwgNo 2/2

32/3,AB/13 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013823349
WPI Acc No: 2001-307561/200132
Related WPI Acc No: 2002-236895
XRAM Acc No: C01-094851
XRPX Acc No: N01-220105

Formation of package for mounting **Ball Grid Array** chips, by creating interconnect layers on top of dielectric layer using Build Up Multilayer technology, and patterning the interconnects to create metal interconnect patterns

Patent Assignee: THIN FILM MODULE INC (THIN-N)
Inventor: HO C W
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6221693	B1	20010424	US 99332427	A	19990614	200132	B

Priority Applications (No Type Date): US 99332427 A 19990614

Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 6221693 B1 10 H01L-021/48
Abstract (Basic): US 6221693 B1
Abstract (Basic):

NOVELTY - A package is formed by depositing dielectric layer on a substrate, creating interconnect layers on top of the dielectric layer using Build Up Multilayer technology, and patterning the interconnects to create metal interconnect patterns.

DETAILED DESCRIPTION - Formation of a package for mounting of at least one row of **Ball Grid Array** (**BGA**) chips involves providing a metal substrate having a coefficient of thermal expansion (CTE) and first and second surfaces. The first surface of the metal substrate is cleaned. A first layer of dielectric having a CTE is deposited over the first surface. A thin film interconnect layer (56, 58) is deposited over the first dielectric layer forming the first layer of an interconnect substrate. The first layer of interconnect substrate comprises a partially exposed second dielectric layer, and copper **contact pads**. A first Build Up Multilayer (BUM) layer (62) is created over the thin film interconnect layer forming a second layer of interconnect substrate comprising a partially exposed third dielectric layer and copper **contact pads**. A second BUM layer (60) is created over the first BUM layer forming a third layer of interconnect substrate comprising a partially exposed fourth dielectric layer and copper **contact pads**. The second BUM layer is coated with **solder** mask. The metal pads within the second BUM layer are exposed creating openings for **BGA solder connections**. The second surface of the metal substrate is masked and etched creating opening(s) (32) for the insertion of **BGA** chip(s) and exposing portions of the first dielectric layer within the openings. Openings are created in the exposed first dielectric layer providing electrical access to the interconnect substrate for the **BGA** chip(s). The metal substrate is subdivided into individual **BGA** substrate.

USE - The method is used for forming a package for mounting of at least one row of **Ball Grid Array** chips. It can also be used to Land Grid Array and Pin Grid Array devices.

ADVANTAGE - The method is inexpensive and reduces performance limitations imposed by prior art high-density flip chip **BGA** manufacturing techniques. It provides for high pin fan-out for flip chip **BGA** devices, and eliminates the need for counter-balancing the effects of thick dielectric layers. It also provides a structure devoid of warpage and dimensional variations during **high temperature** or wet chemical processing for the creation of high density flip chip BGAA structures.

DESCRIPTION OF DRAWING(S) - The figure shows a multichip package with four interconnect layers.

Opening (32)
Film interconnect layers (56, 58)
Second BUM layer (60)
First BUM layer (62)
pp; 10 DwgNo 4/6

32/3,AB/14 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013683833
WPI Acc No: 2001-168046/200117

Related WPI Acc No: 2003-669518
XRAM Acc No: C01-050065
XRPX Acc No: N01-121187
Fabrication of multilayer microelectronic interconnect structure used in high density interconnects for high performance microelectronic device chips uses a low dielectric constant material, e.g. air as the intralevel dielectric
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: BUCHWALTER L P; CALLEGARI A C; COHEN S A; GRAHAM T O; HUMMEL J P; JAHNES C V; PURUSHOTHAMAN S; SAENGER K L; SHAW J M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6184121	B1	20010206	US 9752174	P	19970710	200117	B
			US 98112919	A	19980709		

Priority Applications (No Type Date): US 9752174 P 19970710; US 98112919 A 19980709
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6184121	B1		18	H01L-021/4763	Provisional application US 9752174

Abstract (Basic): US 6184121 B1
Abstract (Basic):
NOVELTY - A multilayer microelectronic interconnect structure is fabricated by using a low dielectric constant material, e.g. air as the intralevel dielectric which reduces intralevel capacitance.
DETAILED DESCRIPTION - A multilayer microelectronic interconnect structure is fabricated by (i) applying a double layer thickness of a thermally stable and easily processable dielectric material (20, 30) having a top layer and a lower layer on a semiconductor wafer (10); (ii) patterning and etching trenches for wiring tracks on the top layer and vias in the lower layer; (iii) depositing a thin electrically conductive barrier/adhesion layer (60) in the trenches and vias and overfilling the trenches and vias with a thick conductive wiring layer metal; (iv) planarizing the wiring layer metal by etching or polishing to achieve a coplanar inlaid structure of conductors and vias embedded as metal features in the dielectric material;
(v) repeating steps (i-iv) until a requisite number of wiring levels in the interconnect structure are fabricated;
(vi) removing the dielectric metal from all areas of the wafer not directly covered by the conductors by means of an etching process while leaving the dielectric material intact under the metal feature;
(vii) optionally applying a thin conformal passivation layer (100) to cap and protect the exposed metal features;
(viii) annealing the etched structure at an **elevated temperature** in a reducing atmosphere to mitigate any plasma process induced damage;
(ix) laminating a thin taut insulating cover layer (120) to the top surface of the passivated metal features;
(x) optionally depositing a thin insulating environmental barrier layer (130) on top of the cover layer;
(xi) etching terminal vias in the optional barrier layer, insulating cover layer, and the thin conformal passivation layer to provide access for terminal **pad contacts**; and
(xii) depositing and patterning terminal metal pads at the via locations to complete the interconnect structure.
USE - For use in high density interconnects for high performance microelectronic device chips, e.g. for logic, memory, communication, and microcontroller applications.

ADVANTAGE - The i structure possesses a very low capacitance and fast propagation speeds.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic sketch of the interconnect structure after terminal vias have been etched and terminal pads are deposited to complete the fabrication of the structure.

Semiconductor wafer (10)
Double layer of dielectric material (20, 30)
Thin electrically conductive barrier/adhesion layer (60)
Thin conformal passivation layer (100)
Thin taut insulating cover layer (120)
Thin insulating environmental barrier layer (130)
pp; 18 DwgNo 4D/7

32/3,AB/15 (Item 14 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013595385
WPI Acc No: 2001-079592/200109
Related WPI Acc No: 2001-218083
XRAM Acc No: C01-022801
XRPX Acc No: N01-060555

Formation of a stress release contact system in an integrated circuit involves using a leveling plate at **elevated temperature** causing the posts to tilt relative to the wafer surface and be encapsulated in an elastomer

Patent Assignee: LIN M (LINM-I)
Inventor: LIN M
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6159773	A	20001212	US 99249252	A	19990212	200109	B
TW 485505	A	20020501	TW 99123094	A	19991228	200318	

Priority Applications (No Type Date): US 99249252 A 19990212
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6159773	A		9	H01L-021/44	
TW 485505	A			H01L-021/60	

Abstract (Basic): US 6159773 A
Abstract (Basic):

NOVELTY - A stress release contact system is formed in an integrated circuit through application of force to a leveling plate at **elevated temperature**, causing the posts to tilt relative to the wafer upper surface and be encapsulated in an elastomer. An orthogonal spiral that acts as a coil spring to absorb stress originating at the **solder ball** is formed.

DETAILED DESCRIPTION - Formation of a stress release contacting system in an integrated circuit comprises (a) providing a silicon wafer containing a completed integrated circuit and having an upper surface on which **contact pads** are **connected**; (b) forming first metal posts (21), **attached** one-on-one to the **contact pads** and extending vertically upward from the pads; (c) placing a leveling plate on the metal posts; (d) through application of force to the leveling plate at an **elevated temperature**, causing the posts to tilt at an angle relative to the wafer upper surface and to point in a direction; (e) filling all empty spaces between the leveling

plate and the wafer surface with an elastomer (42) while leaving all ends of the posts uncovered; (f) removing the leveling plate; (g) forming a second metal posts (22) that **attach** one-on-one to the uncovered ends; (h) placing a leveling plate on the metal posts; (i) through application of force to the leveling plate at an **elevated temperature**, causing the posts to tilt at the angle relative to the wafer upper surface and to point in a direction which is orthogonal to the direction of the most recently formed posts; (j) repeating steps (e) through (i) several times; (k) filling all empty spaces between the leveling plate and the wafer surface with an elastomer (43) while leaving all ends of the posts uncovered; (l) removing the leveling plate; (m) forming underlayer barrier metal pads (61) on all uncovered ends of the posts; and (n) forming **solder balls** (62) that extend upwards and are **attached** to the underlayer barrier metal pads.

USE - For the formation of a stress release contacting system.

ADVANTAGE - The method provides a structure that absorbs stress between integrated circuits package and semiconductors.

DESCRIPTION OF DRAWING(S) - The figure shows a silicon wafer.

Metal posts (21, 22)

Elastomer (42, 43)

Underlayer barrier metal pads (61)

Solder balls (62)

pp; 9 DwgNo 6/9

32/3,AB/16 (Item 15 from file: 350)

DIALOG(R)File 350:Derwent WPIX

013359332

WPI Acc No: 2000-531271/200048

XRAM Acc No: C00-158218

XRPX Acc No: N00-392798

Integrated circuit packaging involves positioning substrate mounted with chip, in mold to align substrate opening with mold opening, and injecting encapsulant via openings to fill in cavity bounded with chip

Patent Assignee: LSI LOGIC CORP (LSIL-N)

Inventor: ALAGARATNAM M; CHIA C J; LIM S S

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6081997	A	20000704	US 97911418	A	19970814	200048	B

Priority Applications (No Type Date): US 97911418 A 19970814

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6081997	A		7	H05K-003/30	

Abstract (Basic): US 6081997 A

Abstract (Basic):

NOVELTY - Integrated circuit or chip (12) is mounted upon substrate (14) such that **solder bumps** (16) of chip are brought into **contact** with corresponding bonding **pads** of substrate. Then mounted chip is positioned within mold in the state of aligning opening (18) of substrate with mold opening (22) and ejecting encapsulant through openings under pressure to fill in cavity bounded with chip.

DETAILED DESCRIPTION - The **solder bumps** are arranged in two dimensional arrays on underside surface of chip. Bonding pads are arranged in two dimensional arrays on upper surface of substrate. The

opening of substrate is located substantially in the center and extends from upper and under side surfaces. The substrate mounted with chip is placed on planar upper surface of a primary mold (20) such that opening of substrate aligns with primary mold opening. When IC chip and substrate are bonded together the surface of substrate remains parallel to surface of chip, and substrate and mold openings extends along a common axis perpendicular to surfaces of substrate chip. A secondary mold (26) having a cavity (28), is placed above primary mold such that substrate mounted with chip resides within cavity. Air vents (30a,30b) are formed between secondary mold and adjacent portion of substrate and primary mold. The liquid encapsulant comprising **thermally conductive** and electrically insulated particles such as silica filled epoxy, is injected through opening under pressure. Then, the bonded substrate and chip are enveloped by the injected encapsulant. The substrate comprises fiber glass epoxy printed circuit board material or ceramic material such as **aluminum** oxide or **aluminum** nitride. An INDEPENDENT CLAIM is also included for integrated circuit packaging system.

USE - For packaging integrated circuit e.g. microprocessor.

ADVANTAGE - Since the encapsulant envelops the **connections** between integrated circuit and substrate and sides of circuit, they are protected from contaminants e.g. mass line, electrically conductive particles, etc., additional mechanical resistance to movement of circuit relative to substrate is attained. Since injection of liquid is performed under pressure, amount of time required to dispense liquid is reduced, and number of voids present in liquid is also reduced resulting in increase in reliabilities of **solder bump connections**.

DESCRIPTION OF DRAWING(S) - The figure shows the cross-sectional explanatory view of packaging process.

Integrated circuit (12)
Substrate (14)
Solder bump (16)
Openings (18,22)
Primary mold (20)
Secondary mold (26)
Cavity (28)
Air vents (30a,30b)
pp; 7 DwgNo 1/3

32/3,AB/17 (Item 16 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012913838
WPI Acc No: 2000-085674/200007
XRAM Acc No: C00-023903
XRPX Acc No: N00-067168
Thermally enhanced tape **ball grid array** package
Patent Assignee: LSI LOGIC CORP (LSIL-N)
Inventor: CHIA C J; LIM S; LOW O H
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6002169	A	19991214	US 9897883	A	19980615	200007	B

Priority Applications (No Type Date): US 9897883 A 19980615
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6002169	A		5	H01L-023/48	

Abstract (Basic): US 6002169 A

Abstract (Basic):

NOVELTY - Holes are arranged in an array pattern through a tape substrate to expose conductive metal traces on the substrate top. A nonconductive stiffener frame is **attached** to the substrate bottom and has through holes corresponding to those in the substrate. An IC mounted on the substrate is electrically **connected** to the traces. **Solder balls** are **attached** to the exposed traces to allow electrical **connection** of the package to a printed circuit board (PCB).

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a stiffener frame for use in the package, comprising **aluminum** that has been anodized to form a protective insulating coating. The stiffener frame dissipates heat produced by the IC.

USE - The anodized **aluminum** frame serves the dual purpose of supporting the tape automated bonding (TAB) substrate during assembly and dissipating heat generated by the IC chip package.

ADVANTAGE - Improved thermal performance, and thus improved device reliability.

DESCRIPTION OF DRAWING(S) - The drawing shows a section of the **thermally enhanced** tape **ball grid array** package.

traces (115)
solder ball pad (117)
IC **contact pads** (123)
solder balls (125)
substrate holes (130)
wire bonding (140)
encapsulant (145)
stiffener frame (155)
pp; 5 DwgNo 2/3

36/3,AB/1 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03475958
E.I. Monthly No: EI9209112317
Title: What's new in flex circuits.
Author: Schriefer, Nancy
Corporate Source: Prism Marketing Inc, St. Paul, MN, USA
Source: Printed Circuit Fabrication v 15 n 2 Feb 1992 p 52-53
Publication Year: 1992
CODEN: PCFAE6 ISSN: 0274-8096
Language: English
Abstract: The author reports on a technology that mounts bare, unpacked chips directly on flex circuits. The Flip-On-Flex process provides a compact package that further enhances the space-saving attributes inherent in flex circuits. Due to the nature of the flexible substrate, the package shows excellent resistance to cracking during temperature cycling. Chips for the Flip-On-Flex process are made with **solder bumps** that can be located anywhere on the **dice**. Novaclad, a polyimide substrate, needs no **adhesive** for laminating **copper** foil, thereby enabling it to withstand **high temperatures**. A **solder** mask technique is used to apply **solder** paste on the flex circuit's **contact pads**, the **dice** are placed on the pads with optical registration, and a standard reflow **solder** process surface mounts the ICs. The package is **sealed** with epoxy.

36/3,AB/2 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

016135490
WPI Acc No: 2004-293366/200427
XRAM Acc No: C04-112267
XRPX Acc No: N04-232929
Tape automated bonding package structure for e.g. flip chips, comprises tape carrier having tape, leads and heat sink, chip having bonding **pads**, electrical **contacts** and plastic package body
Patent Assignee: VIA TECHNOLOGIES INC (VIAT-N); HO K (HOKK-I); KUNG M (KUNG-I)
Inventor: HO K; KUNG C; KUNG M
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20040042185	A1	20040304	US 2003248554	A	20030129	200427	B
TW 559959	A	20031101	TW 2002120048	A	20020903	200427	

Priority Applications (No Type Date): TW 2002120048 A 20020903
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20040042185	A1		13	H05K-007/02	
TW 559959	A			H01L-021/56	

Abstract (Basic): US 20040042185 A1
Abstract (Basic):
NOVELTY - A tape automated bonding package structure comprises a tape carrier having a tape, leads, and a heat sink; a chip having an active surface provided with bonding **pads**; electrical **contacts** placed between the bonding pads and inner leads; and a

plastic package body encapsulating the chip and tape carrier into an integrated unit.

DETAILED DESCRIPTION - A tape automated bonding (TAB) package structure comprises a tape carrier including a tape (402) with a device opening and outer lead openings, leads, each having inner and outer lead sections (408a, 408b), with the outer leads being exposed through the outer lead openings, and a first heat sink (408c) provided on the tape in a position corresponding to the device opening; a chip (500) having an active surface provided with bonding **pads** (502); electrical **contacts** (504) placed between the bonding pads and inner leads; and a plastic package body encapsulating the chip and tape carrier into an integrated unit.

An INDEPENDENT CLAIM is also included for fabrication of TAB package by **attaching** a tape to a conductive layer having bumps; removing a portion of conductive layer to form a first heat sink and leads, with the first heat sink, the leads, and the tape forming a tape carrier; placing a chip on the tape carrier and **conducting** a **thermal** compression operation; and integrating to encapsulate the chip and tape carrier into an integrated unit.

USE - For e.g. flip chips.

ADVANTAGE - The inventive TAB package has a reduced overall thickness and allows direct electrical **connection** between a wire-bond chip and a lead frame without any intermediate redistribution circuits. This reduces overall circuit length and attenuates problems caused by parasitic inductance. The TAB package provides shorter circuit path with improved electrical performance. The heat sink at the back of the chip provides good electromagnetic shield for the TAB package. Since the tape carrier and the chip are not joined by **solder** material, bump pitch can be reduced to 45 microns.

DESCRIPTION OF DRAWING(S) - The figure is a schematic cross-sectional view of TAB package fabrication.

Tape (402)
Inner and outer lead sections (408a, 408b)
First and second heat sinks (408c, 600)
Nickel/gold layer (416)
Chip (500)
Bonding pads (502)
Electrical contacts (504)
Adhesive glue **layer** (506)
Integrated device package (508)
pp; 13 DwgNo 4F/6

36/3,AB/3 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015661105
WPI Acc No: 2003-723292/200369
XRAM Acc No: C03-199177
XRPX Acc No: N03-578339
Metal structure manufacture for an IC **contact pad** by cleaning a **copper** metallization layer exposed by a window using solvents and plasma treatments, depositing **copper** on the pad, plasma passivating and depositing **copper** stud
Patent Assignee: TEXAS INSTR INC (TEXI); BOJKOV C P (BOJK-I); COFFMAN P (COFF-I); SMITH P B (SMIT-I)
Inventor: BOJKOV C P; COFFMAN P; SMITH P B
Number of Countries: 031 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 1321982	A2	20030625	EP 2002102839	A	20021219	200369 B
US 20030116845	A1	20030626	US 2001342949	P	20011221	200370
			US 200286117	A	20020226	

Priority Applications (No Type Date): US 200286117 A 20020226; US 2001342949 P 20011221

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1321982	A2	E	10	H01L-023/485	
	Designated States (Regional): AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI SK TR				
US 20030116845 A1			10	H01L-023/52	Provisional application US 2001342949

Abstract (Basic): EP 1321982 A2

Abstract (Basic):

NOVELTY - A metal structure for a **contact pad** of an integrated circuit (IC) has a **copper** interconnecting metallization protected by an overcoat.

DETAILED DESCRIPTION - The metal structure comprises a window in the overcoat exposing a portion of the **copper** metallization layer with a clean surface. A patterned **copper** layer is directly positioned on the clean **copper** metallization to give a metal structure with about the same conductivity as pure **copper**. The **copper** layer overlaps the perimeter of the overcoat window and a **copper** stud is positioned on the **copper** layer and follows the contours of the **copper** layer.

Preferred metal structure: The **copper** stud is as wide as the **copper** layer, following the contour of the perimeter of the overcoat window.

An INDEPENDENT CLAIM is also included for a method of cleaning the surface of **copper** metallization IC interconnection and exposed to **contact pads** comprising:

(1) removing organic contamination and particles from the wafer **copper contact pads** and drying;

(2) exposing the wafer to an oxygen and nitrogen/argon/helium plasma, to ash any organic residue and to oxidize the **copper** surface to a controlled thickness;

(3) still under vacuum, exposing the wafer to a hydrogen and nitrogen/helium/argon plasma to remove the formed **copper** oxide from the pad surface and to passivate the cleaned surface;

(4) sputtering-**etching** the passivated pad surface with energetic ions to simultaneous create a fresh surface and activate it;

(5) sputter-depositing a layer of **copper** covering the fresh pad surface and pad perimeter;

(6) exposing the wafer again to a hydrogen and nitrogen/argon plasma to passivate the **copper** layer; and

(7) depositing a **copper** stud onto the **copper** layer without contaminating the passivated **copper** layer.

Preferred method: The solvent cleaning step preferably comprises immersing the wafer in agitated isopropyl alcohol, methanol, glycol, N-methyl pyrrolidine, etc., subjecting to ultrasound energy, spraying the wafer with an organic solvent and treating the wafer in a dry chemical vapor.

A **solder bump** is preferably deposited onto the **copper** stud.

USE - For fabrication of metal bumps for flip-chip assembly of semiconductor chips.

ADVANTAGE - The **contact pad copper pad** -layer is deposited directly on the integrated circuit (IC)

copper metallization without any intermediate barrier layer so that the resulting minimum **electrical** resistance **enhances** the high speed performance of the IC.

The process and reliability of wafer-level functional probing by eliminating probe marks and subsequent plating difficulties.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross section of a **solder bump** with **copper** seed layer and **copper** stud over the chip **contact pad** metallization.

Contact pad (500)
Copper layer (501)
Window (501a)
Insulating material (502)
Overcoat (503)
Overcoat overlap (503a)
Polymer overcoat layer (506)
Overcoat slope (506a)
Copper layer (507)
Copper stud (508)
Solder bumps (509)
pp; 10 DwgNo 5/6

36/3,AB/4 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015607896
WPI Acc No: 2003-670053/200363
Related WPI Acc No: 2003-166122
XRAM Acc No: C03-182631
XRPX Acc No: N03-534958
Ball grid array package for packaging an Integrated Circuit **die** in cavity has substrate containing three layers with second openings
Patent Assignee: ST ASSEMBLY TEST SERVICES LTD (STAS-N)
Inventor: AQUIEN W; BRIAR J; FEE S S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030085462	A1	20030508	US 2001849671	A	20010507	200363	B
			US 2002323447	A	20021219		

Priority Applications (No Type Date): US 2001849671 A 20010507; US 2002323447 A 20021219
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030085462	A1		9	H01L-023/34	Div ex application US 2001849671 Div ex patent US 6537857

Abstract (Basic): US 20030085462 A1
Abstract (Basic):

NOVELTY - A **ball grid array** package for packaging an Integrated Circuit (IC) **die** (12) in a cavity comprises a substrate layer (20) with three layers, a heat sink (10) with a cavity, first and second **adhesive layers** (18), wire bond **connections**, and **solder balls**. The two **adhesive layers attach** the IC **die** to the heatsink. The wire bond **connection** is in between the IC **die** and the substrate layer.

DETAILED DESCRIPTION - A **ball grid array** package

for packaging an IC **die** (12) in a cavity comprises a substrate layer (20) with three layers, a heat sink (10) with a cavity (16), first and second **adhesive layers** (18), wire bond **connections**, and **solder balls**. The cavity in the heatsink has a bottom with a surface, and sidewalls. The two **adhesive layers attach** the IC **die** to the heatsink. The wire bond **connection** is in between the IC **die** and the substrate layer. The IC has a bottom surface, sidewalls and a ground point.

USE - As a **ball grid array** package for packaging an Integrated Circuit **die** in cavity.

ADVANTAGE - The method enables a low-resistivity short wire bond **connection** between a ground point of the integrated circuit **die** and the heatsink. It is inexpensive and simple.

DESCRIPTION OF DRAWING(S) - The figure shows a cross section in an X-direction of the package.

Heat sink (10)
Cavity (16)
Adhesive layers (18)
Substrate layer (20)
Lower (22)
Center (24)
Upper layer (26)
Solder mask layer (27)
Copper traces (38)
pp; 9 DwgNo 2a/2

36/3,AB/5 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015417478
WPI Acc No: 2003-479618/200345
XRAM Acc No: C03-128182
XRPX Acc No: N03-381203
Reel-to-reel tape, having first and second surfaces, useful in assembly of semiconductor chips, comprises contact lands and electrically conductive routing lines, and chip mount pad
Patent Assignee: ANO K (ANOK-I)
Inventor: ANO K
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030034553	A1	20030220	US 2001930361	A	20010815	200345	B

Priority Applications (No Type Date): US 2001930361 A 20010815
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030034553	A1		9	H01L-023/48	

Abstract (Basic): US 20030034553 A1
Abstract (Basic):

NOVELTY - A reel-to-reel tape (201), having first and second surfaces (201a, 201b), useful in the assembly of semiconductor chips, comprises contact lands (205c) and electrically conductive routing lines integral with the first surface of the tape, and a chip mount pad, **secured** to the first surface, coplanar with the second surface.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the

following:

(a) a low-profile, high power semiconductor device including a plastic tape having a first and second surfaces, a portion of the first surface covered with an **adhesive layer**, comprising first and second openings through the tape and **adhesive layer**, where the first opening configured to **solder balls**, and the second opening is configured to accommodate circuit chips; a **copper** foil laminated on the **adhesive layer**; portions of the **copper** foil in the second opening is mechanically shaped into a position coplanar with the second surface, for use as chip mount pads; circuit chips mounted using a **thermally conductive** material on each of the chip mount pads; and encapsulating material (208) surrounding the mounted chips;

(b) the production of a reel-to-reel assembly tape having first and second surfaces, the first surface having an **adhesive layer** on it, for use in the assembly of semiconductor devices, comprising punching the first and second openings through the tape and **adhesive layer**, the first openings configured to **solder balls**, and the second openings configured to accommodate the chips; laminating a **copper** foil on the **adhesive layer**; and mechanically shaping portions of the **copper** foil into the second openings, positioning the portions in the same plane as the second surface; and

(c) the production of a low profile, high power semiconductor device, comprising providing a reel-to-reel plastic tape having first and second surfaces and at least a portion of the first surface covered with an **adhesive layer**; punching first and second openings as above, through the tape and **adhesive layer**; laminating a **copper** foil on the **adhesive layer**; photolithography patterning and chemically **etching** the **copper** foil, creating routing lines and **contact pads**; mechanically shaping portions of the **copper** foil into the second openings, bending the foil to become coplanar with the second surface; and protecting a portion of the **etched** foil with a **solder** mask while plating the exposed portions with nickel and gold; mounting a circuit chip on each of the chip mount pads; wire bonding the chips to the routing lines; encapsulating the first surface of the tape including each of the mounted chips and bonding wires; and **attaching solder balls** to the surface of the **contact pads** exposed by the first tape openings.

USE - Used in the assembly of semiconductor chips (claimed). The reel-to-reel tape is also used in the field of electronic systems and semiconductor devices, particularly **ball-grid array** devices intended for high power operation.

ADVANTAGE - The reel-to-reel tape **enhances** the **thermal** performance of **ball-grid array** packages without the need for additional, potentially expensive features. It further provides excellent electrical performance, mechanical stability and high reliability.

DESCRIPTION OF DRAWING(S) - The figure shows a magnified cross-section of a portion of an actual device illustrating the key features of the reel-to-reel tape.

Reel-to-reel tape (201)
First and second surfaces (201a, 201b)
Contact lands (205c)
Encapsulating material (208)
pp; 9 DwgNo 2/16

36/3,AB/6 (Item 5 from file: 350)

DIALOG(R)File 350:Derwent WPIX

014821283
WPI Acc No: 2002-641989/200269
XRAM Acc No: C02-181274
XRPX Acc No: N02-507397
Fabrication of integrated circuit package for **ball grid** arrays, involves forming three-layer carrier by laminating layers of fiberglass prepreg and **copper** foil to **copper** plate
Patent Assignee: ASAT LTD (ASAT-N)
Inventor: FAN C H; LAU P L; MCLELLAN N; TSANG K C
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020068378	A1	20020606	US 2000730440	A	20001205	200269	B
US 6429048	B1	20020806	US 2000730440	A	20001205	200269	

Priority Applications (No Type Date): US 2000730440 A 20001205
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020068378	A1		8	H01L-021/44	
US 6429048	B1			H01L-021/44	

Abstract (Basic): US 20020068378 A1
Abstract (Basic):

NOVELTY - An integrated circuit package is fabricated by laminating layers of fiberglass prepreg and **copper** foil to a **copper** plate to form a three-layer laminated carrier; patterning and **etching contact pads** for input/output and a power/ground ring; applying **solder** mask and plating up the **contact pads** and ring with wire bondable metal surface; and forming window openings for receiving **dies**.

DETAILED DESCRIPTION - Fabrication of integrated circuit package for **ball grid** arrays involves laminating layers of fiberglass prepreg and **copper** foil to a **copper** plate to form a three-layer laminated carrier; patterning and **etching contact pads** for input/output and a power/ground ring; applying a **solder** mask and plating up the **contact pads** and the ring with a wire bondable metal surface; and forming window openings for receiving semiconductor **dies**. The **dies** are then **attached** within the windows, wire bonded to the **contact pads** and the ring, and encapsulated. **Solder balls** are **attached** to the **contact pads** to form finished packages. The finished packages are singulated into individual packages, and the **copper** plate portion of each of the individual packages is then **attached** to **copper** plate **heat spreader**.

USE - For fabricating an integrated circuit package for **ball grid** arrays.

ADVANTAGE - The inventive method provides a package which eliminates the requirement for expensive polyimide tape. The accuracy of the artwork relative to the **die attach** cavity is an inherent feature of the way the package is fabricated. This precludes any alignment inaccuracies of tape to heat sink **attachment** which can cause problems in prior art.

DESCRIPTION OF DRAWING(S) - The figure illustrates the formation of the window opening during fabrication of the integrated circuit package.

pp; 8 DwgNo 8B/10

36/3,AB/7 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013796913
WPI Acc No: 2001-281125/200129
Related WPI Acc No: 2001-272598
XRAM Acc No: C01-085410
XRPX Acc No: N01-200441
Semiconductor and flip chip packages, uses thermo-electrically conductive epoxy resin to **connect** bond pad to backside of **die**
Patent Assignee: MINCO TECHNOLOGIES LABS INC (MINC-N); MINCO TECHNOLOGY LABS INC (MINC-N)
Inventor: POTTER D R; RODENBECK L R
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20010000927	A1	20010510	US 9865677	A	19980423	200129 B
			US 2000739071	A	20001218	
US 6406938	B2	20020618	US 9865677	A	19980423	200244
			US 2000739071	A	20001218	

Priority Applications (No Type Date): US 9865677 A 19980423; US 2000739071 A 20001218
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010000927	A1		9	H01L-023/48	Div ex application US 9865677 Div ex patent US 6191487
US 6406938	B2			H01L-021/44	Div ex application US 9865677 Div ex patent US 6191487

Abstract (Basic): US 20010000927 A1
Abstract (Basic):
NOVELTY - A via (22) electrically **connects** the terminal and the **contact pad** (21) on the external (19) and internal (17) sides of the substrate (18) respectively. A **die** (12) is positioned so that its front side faces the substrate external side. A metallisation layer (26) is formed on the back side (28) of the **die**. A bond pad (16) between the **die** and substrate mates with the **contact pad**. A conductive substance (20) **connects** the **die** back side to the bond pad to form an electrical **connection** from the **die** back side to the substrate terminal.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the manufacture of a flip chip package, a semiconductor chip package, and the manufacture of a semiconductor package.

USE - Manufacturing and **connecting** semiconductor and flip chip packages to printed circuit boards using a back side **connection**.

ADVANTAGE - The area required for both discrete devices and integrated circuits formed from a standard **die** having back side **connections** is reduced. There is no need for lead wires extending from the **die** in a flip chip package to the printed circuit board so reducing the space require to **connect** the device to the remainder of the circuit.

DESCRIPTION OF DRAWING(S) - The drawing shows a side cross-section of the flip chip package.

Die (12)
Potting material (14)

Bond pad (16)
Internal sides of the substrate (17)
Substrate (18)
External side of the substrate (19)
Conductive substance (20)
Contact pad (21)
Via (22)
Solder balls (24)
Metallisation (26)
Back side of the **die** (28)
pp; 9 DwgNo 1/5

36/3,AB/8 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008286007
WPI Acc No: 1990-173008/199023
XRPX Acc No: N90-134549
Self regulating temp. **heater** with **thermally conductive** extensions - has current return path and source for selectively passing AC through heater body and path
Patent Assignee: AMP INC (AMPI); WHITAKER CORP (WHIT-N)
Inventor: HENSCHEN H E; MCKEE M J; PAWLIKOWSKI J M; PAWLIKOWSK J M
Number of Countries: 009 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 371646	A	19900606	EP 89311663	A	19891110	199023	B
JP 2187263	A	19900723	JP 89307781	A	19891129	199035	
US 5059756	A	19911022	US 88277116	A	19881129	199145	
CA 1310137	C	19921110	CA 612942	A	19890925	199251	
EP 371646	B1	19940309	EP 89311663	A	19891110	199410	
DE 68913666	E	19940414	DE 613666	A	19891110	199416	
			EP 89311663	A	19891110		
JP 2719970	B2	19980225	JP 89307781	A	19891129	199813	
KR 155358	B1	19981215	KR 8917347	A	19891128	200034	

Priority Applications (No Type Date): US 88277116 A 19881129
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 371646	A				
Designated States (Regional): DE FR GB IT NL					
CA 1310137	C			B23K-003/04	
EP 371646	B1	E	24	B23K-003/04	
Designated States (Regional): DE FR GB IT NL					
DE 68913666	E			B23K-003/04	Based on patent EP 371646
JP 2719970	B2		16	B23K-003/04	Previous Publ. patent JP 2187263
KR 155358	B1			H05B-001/02	

Abstract (Basic): EP 371646 A
Spaced **contact pads** (23) on a printed circuit board (19) are **soldered** to respective spaced contacts (21) in a cable or **connector** assembly by means of respective spaced **connecting** members (15) interposed between contacts (21) to be **soldered**. The **connecting** members (15) are electrically and **thermally conductive** finger-like projections formed as part of a heater body (10) and are severable from the heater body (10) after **soldering** to thereby remain part of the final **solder connection**. A prescribed amount of fusible material (e.g., **solder**) is pre-deposited on the **connecting** members (15) or

contacts (21) and is melted when the heater is actuated.

The heater body (10) is a self-regulating heater in the form of a **copper** substrate (11) having a thin surface layer (13) of magnetically permeable, high resistance alloy. An alternating current of constant amplitude and high frequency is passed through the heater body (10) and is concentrated in the surface layer at temperatures below the surface layer Curie temperature.

USE - Joining flexible **etched** cables, ribbon cables and surface mount **connectors**. (24pp Dwg.No.1/19)

Abstract (Equivalent): EP 371646 B

A tool for providing thermal energy to at least one electrical **connection** site for providing an electrically conductive **connection** between first and second electrically conductive contacts (21,23) to **connect** said contacts (21,23) to each other at the, or each, such site, the tool being of the type adapted to generate sufficient thermal energy until achieving a preselected temperature to **melt** a fusible **conductive** material for providing said **connection** between said contacts (21,23), and having a selectively actuable heater body (10) for supplying the thermal energy, which has a substrate (11) of an electrically-conductive first material having a relatively low electrical resistivity and relatively low magnetic permeability, and a skin layer (13) of an electrically-conductive second material disposed on at least a portion of a first surface of said substrate (11) and having a higher electrical resistivity than that of the first material, and having a magnetic permeability which at temperatures below its Curie temperature is substantially greater than said relatively low magnetic permeability and at temperature above its Curie temperature is substantially the same as said relatively low magnetic permeability, characterised in that: said tool includes at least one **thermally-conductive** extension member (15) **secured** to and in **thermally-conductive** contact with said **heater** body (10), the, or each, said extension member (15) being adapted to be disposed in both electrical and thermal engagement with, and physically between, said first contact (23) and said second contact (21) to transfer said sufficient thermal energy to said first and second contacts (21,23) from said heater body (10) and to remain a permanent part of the electrically-conductive **connection** between the first and second contacts (21,23) while said substrate (11) is either inherently electrically isolated from, or is adapted to be electrically isolated from, the, or each, such **connection**.

(Dwg.1/19

Abstract (Equivalent): US 5059756 A

Spaced **contact pads** (23) on a printed circuit board (19) are **soldered** to respective spaced contacts (21) in a cable or **connector** assembly by respective spaced **connecting** members (15) interposed between contacts to be **soldered**. The **connecting** members are electrically and **thermally conductive** finger-like projections formed as part of a heater body (10) and are readily severably from the body after **soldering** to remain part of the final **solder connection**. A prescribed amount of fusible material e.g., **solder** is pre-deposited on the **connecting** members and/or contacts and is melted when the heater is actuated. The heater body may be a self-regulating heater in the form of a **copper** substrate (11) having a thin surface layer (13) of magnetically permeable, high resistance alloy. An alternating current of constant amplitude and high frequency is passed through the heater body and is concentrated in the surface layer at temperatures below the surface layer Curie temperature. ADVANTAGE - Reduces risk of **solder** bridging between **connection** sites.

(24pp

36/3,AB/9 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

003903875
WPI Acc No: 1984-049420/198408
XRAM Acc No: C84-020852
XRPX Acc No: N84-037490
Stitching pad for changing **connections** on PCB - comprising bonded **polyepoxy resin layer** and metal **layer** welded to **connecting** wire
Patent Assignee: BURROUGHS CORP (BURS); WERY M J C (WERY-I)
Inventor: JEHAY M; WERY M J
Number of Countries: 007 Number of Patents: 014
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 8400664	A	19840216				198408 B
GB 2124835	A	19840222	GB 8222359	A	19820803	198408
EP 114857	A	19840808	EP 83902435	A	19830802	198432
GB 2155368	A	19850925	GB 856525	A	19850313	198539
GB 2155382	A	19850925	GB 856524	A	19850313	198539
GB 2124835	B	19860430				198618
GB 2155368	B	19860723				198630
GB 2155382	B	19860723				198630
EP 206063	A	19861230	EP 83107771	A	19830802	198652
US 4654102	A	19870331	US 86867908	A	19860520	198715
EP 114857	B	19880330				198813
DE 3376187	G	19880505				198819
EP 206063	B	19890719				198929
DE 3380247	G	19890824				198935

Priority Applications (No Type Date): GB 8222359 A 19820803; GB 856524 A 19820407
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 8400664	A	E	36		
Designated States (National): US					
Designated States (Regional): BE DE FR NL SE					
EP 114857	A	E			
Designated States (Regional): BE DE FR NL SE					
EP 206063	A	E			
Designated States (Regional): BE DE FR NL SE					
EP 114857	B	E			
Designated States (Regional): BE DE FR NL SE					
EP 206063	B	E			
Designated States (Regional): BE DE FR NL SE					

Abstract (Basic): EP 114857 A

A selectively positionable stitching pad (P1,P2) for use in changing electrical **connections** on printed circuit boards (PC), said pad (P1,P2) including a plurality of layers of material (32,34, 36,38) bonded together to form a sandwich structure, one of said layers (32,34,36,38) being a layer of weldable material (38) on a first face of said pad (P1,P2) responsive to application of heat at a first selected level to form a weld with suitable wire (24) placed in **contact** therewith; said **pad** (P1,P2) being characterised by another of said layers (32,34,36,38) being a **layer** of **adhesive** material (32) on a second face of said pad (P1,P2)

responsive to application of heat at a second selected level to **adhere** to a surface (PC) with which it is placed in **contact** to bond the **pad** (P1,P2) to the surface (PC) and to retain the bond during subsequent application of heat.

(17pp

Abstract (Equivalent): EP 114857 B

A selectively positionable stitching pad (P1,P2) for use in changing electrical **connections** on printed circuit boards (PC), said pad (P1,P2) including a plurality of layers of material (32,34, 36,38) bonded together to form a sandwich structure, one of said layers (32,34,36,38) being a layer of weldable material (38) on a first face of said pad (P1,P2) responsive to application of heat at a first selected level to form a weld with suitable wire (24) placed in **contact** therewith; said **pad** (P1,P2) being characterised by another of said layers (32,34,36,38) being a **layer** of **adhesive** material (32) on a second face of said pad (P1,P2) responsive to application of heat at a second selected level to **adhere** to a surface (PC) with which it is placed in **contact** to bond the **pad** (P1,P2) to the surface (PC) and to retain the bond during subsequent application of heat.

EP 206063 B

A method for changing electrical **connections** on a printed circuit board by **attachment** to the printed circuit board of a pad, the method including providing an electrically conductive weldable layer on a first face of the pad whereto a suitable wire can be welded in response to application of heat at a first predetermined level, and the method being characterised by including the steps of providing a **layer** of heat curable **adhesive** on a second face of the pad responsive to application of heat at a second predetermined level to **attach** the pad to the surface of the printed circuit board to bond the pad to the board and to maintain the pad so bonded during subsequent application of heat, and passing an electric current through the electrically **conductive** weldable layer to **heat** the electrically **conductive** weldable layer for **heat** at the second predetermined level to be applied to the **layer** of heat curable **adhesive**.

Abstract (Equivalent): GB 2124835 B

A method for changing electrical **connections** on a printed circuit board by **attachment** to a printed circuit board of a pad whereto additional electrical **connections** can be made, said method including the steps of: providing a **layer** of heat curable **adhesive** material on a first face of said pad responsive to application of heat at a predetermined level to **attach** said pad to the surface of the printed circuit board to bond said pad to the board and to keep said pad so bonded during subsequent application of **heat**; providing an electrically **conductive** layer on a second face of said pad suitable for having a wire resistance welded thereto by application of a first electrode to the wire to urge the wire into electrical contact with said electrically conductive layer, by application of a second electrode to said electrically conductive layer, and by subsequent passage of electrical charge between said first and second electrodes; and passing of electrical current through said electrically **conductive** layer to **heat** said electrically **conductive** layer for said **heat** at said predetermined level to be applied to said **layer** of **adhesive** material.

GB 2155368 B

An apparatus for correcting printed circuit boards, said apparatus comprising, a pad dispenser, operative to dispense a stitching pad to be **attached** to a printed circuit board, said stitching pad

comprising a heat activated **adhesive layer** on a first face thereof and an electrically conductive weldable layer on a second face thereof; a pad positioner operative to receive a stitching pad from said pad dispenser and to apply said first face of the pad to a selectable location on a printed circuit board; and first and second electrodes operative thereafter to provide electrical contact with said weldable layer, said first and second electrodes being operative thereafter to pass a first electrical current therebetween to cause said weldable layer to generate heat for transfer to said **adhesive layer** to cause said **adhesive layer** to bond the pad to the printed circuit board and to remain so bonded during subsequent heating; where said first electrode is operative thereafter to urge a wire against said weldable layer and said second electrode is operative to provide electrical contact with said weldable layer; and where said first and second electrodes are operative thereafter to pass a second electric current therebetween, to provide an electrical resistance weld between the wire and said weldable layer on the pad.

GB 2155382 B

A method for stitching wire to electrically conductive positionable pads comprising the following steps: positioning a first electrode bearing an insulated wire over a positionable pad; moving a plunger to cause a right angle to be formed in the wire, and thus to position a portion of the wire between the end of said first electrode and the positionable pad; lowering a second electrode associated with said first electrode until the end of said second electrode extends beyond the end of said first electrode in the direction of the pad; lowering said first and second electrodes togehter until said second electrode comes into electrical **contact** with the positionable **pad**; lowering said first electrode until the wire is interposed between the positionable pad and said first electrode; applying a sufficient mechanical force towards the pad to said first electrode to break the insulation on the wire for the wire to have electrical **connection** both with said first electrode and with the pad; initiating current flow between said first and said second electrodes of sufficient magnitude to resistance weld the wire to the surface of the positionable pad; and removing said first and said second electrodes from the positionable pad.

Abstract (Equivalent): WO 8400664 A

Pad comprising a heat responsive **adhesive layer** (**epoxy resin**) and a weldable stitching layer (stainless steel) is placed on the PCB with the **adhesive layer** in contact with the board and heated to bond the **adhesive layer** to the board. A wire (Ni) is then welded to the stitching layer to establish electric **connection**. Optionally the pad may include a plated (**Cu, solder**) through hole to allow **connections** to the existing circuitry on the boards and to components mounted in the holes by flow **soldering**.

The stitching pads can be used for correcting existing standard PCBs.

0/18

US 4654102 A

Changing electrical **connections** on printed circuit boards, comprises the use of positionable pads having a heat responsive **adhesive** side and a stitching side.

A ribbon is advanced along a rigid support and **cut** to produce a pad.

The pad is then moved into a required position **adhesive** side down in contact with the face of a printed circuit board. The pads are heated to cause the pads to **adhere** to the board A wire is placed

in contact with the stitching side of a pad **attached** to the board.

The wire is then welded to the pad to establish the necessary electrical **connections.**

(7pp

40/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010442841
WPI Acc No: 1995-344160/199544
XRPX Acc No: N95-257178
Thick film fuse with high current rating for **PCB** surface mounting - uses fusible gold film printed directly onto ceramic substrate and has covering of arc suppressive glass over fuse element
Patent Assignee: AEM HOLDINGS INC (AEMH-N)
Inventor: MONTGOMERY J D
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5453726	A	19950926	US 93174865	A	19931229	199544	B

Priority Applications (No Type Date): US 93174865 A 19931229
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5453726	A		8	H01H-085/04	

Abstract (Basic): US 5453726 A
The fuse assembly consists of a ceramic substrate which is capable of withstanding **high temperature** processing onto which the thick film bow tie shaped fuse element is screen printed and fired. Terminations of silver are then printed and fired to provide **connections** between fuse element and end caps or external leads. After placement of terminations a thick film of low melting point arc suppressant glass is screen printed or syringed over the fusible element and extends slightly onto the terminations The terminations can be leads or **solder bumps** on the thick film **contact pads** but **copper** alloy end caps allow for greater amperage capacity and isolate the fuse assembly from potential mechanical stresses USE/ADVANTAGE-Allows for ratings in excess of 10 amps. and 32 volts DC, the limits for currently available commercial thin film fuses
Dwg.1b/4

40/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008286006
WPI Acc No: 1990-173007/199023
XRPX Acc No: N90-134548
Self regulating temp. heater as part of **PCB** - generates sufficient thermal energy at surface layer by resistive heating at temp. below Curie temp. of surface layer
Patent Assignee: AMP INC (AMPI); WHITAKER CORP (WHIT-N)
Inventor: HENSCHEN H E; MCKEE M J; PAWLIKOWS J M
Number of Countries: 008 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 371645	A	19900606	EP 89311662	A	19891110	199023	B
JP 2192876	A	19900730	JP 89307784	A	19891129	199036	
US 5010233	A	19910423	US 88277095	A	19881129	199120	
CA 1294375	C	19920114				199209	

Priority Applications (No Type Date): US 88277095 A 19881129

Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
EP 371645 A
Designated States (Regional): DE FR GB IT NL

Abstract (Basic): EP 371645 A
A heater (20) is **secured** to or embedded in a **circuit board** (10) and is selectively energisable by current to melt **solder** in a **connection** or disconnection operation. The heater (20) is spaced from **circuit board contact pads** (13) by **circuit board** structure material that transmits the generated thermal energy to the **contact pads** (13) to melt **solder** or other fusible material. The heater is pref. a self-regulating heater in the form of a **copper** substrate (12) having a thin surface layer (20) of magnetically permeable, high resistance material.

An alternating current of constant amplitude and high frequency is passed through the heater and concentrated in the surface layer (20) at temperatures below the surface layer Curie temp. At **higher temperatures** the current is distributed through the lower resistance substrate (12) to limit further heating. A current return path or bus (21) is disposed in closely-spaced parallel relation to the surface layer (20) and establishes an electric field between the substrate (12) and the return bus (21) to bias current in the substrate toward the surface layer (20).

USE - **Printed circuit board.** (14pp Dwg.No.2/9)

Abstract (Equivalent): US 5010233 A
The heater (20) is **secured** to or embedded in a **circuit board** (10) and is selectively energisable by a current to melt a **solder** in a **connection** or disconnection operation.

The heater is spaced from **circuit board contact pads** (13) by **circuit board** structure material that transmits the generated thermal energy to the **contact pads** to melt the **solder** or other fusible material. The heater is a self-regulating heater in the form of a **copper** substrate having a thin surface layer of magnetically permeable, high resistance material. An alternating current of constant amplitude and high frequency is passed through the heater and concentrated in the surface layer at temperatures below the surface layer Curie temperature.

At **higher temperatures** the current is distributed through the lower resistance substrate to limit further heating. A current return path (21) or bus is disposed in closely-spaced parallel relation to the surface layer and establishes an electric field between the substrate and the return bus to bias current in the substrate toward the surface layer. The return bus may be embedded in the **circuit board** or provided as part of external tooling used to deliver energising current. USE/ADVANTAGE - Self-regulating heater for **connecting** (**soldering**) and disconnecting (unsoldering) applications.

(14pp

40/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008286005
WPI Acc No: 1990-173006/199023
XRPX Acc No: N90-134547
Surface mount technology breakaway self regulating temp. heater - has

solder tails each adapted to be disposed in both electrical and thermal engagement with respective **contact pad** on board

Patent Assignee: AMP INC (AMPI); WHITAKER CORP (WHIT-N); AMP CORP (AMPI)

Inventor: HENSCHEN H E; MCKEE M J; PAWLIKOWSKI J M; PWALIKOWSK J M

Number of Countries: 009 Number of Patents: 007

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 371644	A	19900606	EP 89311649	A	19891110	199023	B
JP 2276181	A	19901113	JP 89307783	A	19891129	199051	
US 5103071	A	19920407	US 88277362	A	19881129	199217	
CA 1310138	C	19921110	CA 612978	A	19890925	199251	
EP 371644	B1	19930811	EP 89311649	A	19891110	199332	
DE 68908362	E	19930916	DE 608362	A	19891110	199338	
			EP 89311649	A	19891110		
KR 150444	B1	19981015	KR 8917349	A	19891128	200026	

Priority Applications (No Type Date): US 88277362 A 19881129

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 371644	A				
Designated States (Regional): DE FR GB IT NL					
US 5103071	A		9		
EP 371644	B1	E	13	B23K-003/04	
Designated States (Regional): DE FR GB IT NL					
DE 68908362	E			B23K-003/04	Based on patent EP 371644
KR 150444	B1			H01R-004/02	
CA 1310138	C			B23K-003/04	

Abstract (Basic): EP 371644 A

Soldering of surface mount **connector** terminals to **contact pads** (41) on **circuit board** (40) is facilitated by configuring the terminals (33) and their **solder** tails (39) as spaced integrally-formed projections of a selectively actuable heater. Thermal energy developed in the **heater** (35) is **conducted** along the projections to the **solder** tails (39) to **melt** fusible **conductive** material (e.g. **solder**, at the **connection** sites). After cooling, the projections are severed from the heater (35).

The terminals (33), which are formed at the distal ends of the projections, are typically supplied partially inserted in respective terminal-receiving passages (31) of the **connector** housing (30). After the **soldering** operation, the terminals (33) are fully inserted into the passages (31). The heater (35) is preferably a self-regulating heater in the form of a **copper** substrate having a skin layer (13) of magnetically permeable, high resistance material.

USE - **PCB**. (10pp Dwg.No.4/6)

Abstract (Equivalent): EP 371644 B

A surface mount **connector** (30) for joining plural individual terminals thereof to respective plural spaced **contact pads** (41) on a **circuit board** (40) surface by providing a sufficient thermal energy to **melt** a fusible electrically-**conductive** material (72,74) at said **contact pads** (41), the **connector** having a selectively actuable heater body (35) for supplying said at least sufficient thermal energy, the body having a substrate of an electrically-conductive first material having a relatively low electrical resistivity and relatively low magnetic permeability, the substrate including a first surface, the substrate having a skin layer of an electrically-conductive second material disposed on at least a portion of the first surface, said second material having a higher electrical resistivity than that of the first

material, and having a magnetic permeability which at temperatures below its Curie temperature is substantially greater than said relatively low magnetic permeability and at temperatures above its Curie temperature is substantially the same as the relatively low magnetic permeability, the **connector** being characterized by a plurality of mutually spaced **thermally-conductive connecting** members **secured** to and in **thermally-conductive** engagement with said **heater** body (35), each of said **connecting** members having a distal end in the form of a respective terminal (33) of the surface mount **connector** (30), a proximal end **secured** to said heater body (35), and an intermediate portion configured as a **solder** tail (39), wherein each of said **solder** tails (39) is adapted to be disposed in both electrical and thermal engagement with a respective **contact pad** (41) on the **circuit board** (40) to transfer said sufficient thermal energy to said respective **contact pad** (41) from said heater body (35) and thereafter remain permanently **connected** to said respective **contact pad** (41).

(Dwg.1/6

Abstract (Equivalent): US 5103071 A

Soldering of surface mount **connector** terminals to **contact pads** on a **circuit board** is facilitated by configuring the terminals and their **solder** tails as spaced integrally-formed projections of a selectively actuable heater. Thermal energy developed in the **heater** is **conducted** along the projections to the **solder** tails to **melt** fusible **conductive** material (e.g., **solder**, at the **connection** sites). After cooling, the projections are severed from the heater. The terminals, which are formed at the distal ends of the projections, are typically supplied partially inserted in respective terminal-receiving passages of the **connector** housing. After the **soldering** operation, the terminals are fully inserted into the passages.

The heater is preferably a self-regulating heater in the form of a **copper** substrate having a skin layer of magnetically permeable, high resistance material. An alternating current of constant amplitude and high frequency is passed through the heater and concentrated in the skin layer at temperatures below the Curie temperature of the skin layer material. At **higher temperatures** the current is distributed through the lower resistance substrate to limit further heating. During the time interval required for the surface layer to reach its Curie temperature, the resistive power dissipation creates **thermal** energy that is **conducted** to the **solder** tails.

40/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004069793
WPI Acc No: 1984-215334/198435
XRPX Acc No: N84-161317
Heat-dissipating chip carrier substrates - consists of electrically-conductive **layer** on top of **elastomeric layer** formed in pattern off contact elements
Patent Assignee: SMITHS IND PLC (SMIS)
Inventor: BALDWIN G J; MCCANN M O
Number of Countries: 003 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2135525	A	19840830	GB 844217	A	19840217	198435	B

FR 2541511	A	19840824					198439
US 4509096	A	19850402	US 84578924	A	19840210		198516
GB 2135525	B	19860618					198625

Priority Applications (No Type Date): GB 834890 A 19830222; GB 834865 A 19830222; GB 844217 A 19840217

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2135525	A		7		

Abstract (Basic): GB 2135525 A

The substrate is formed on a rigid multi-layer **circuit board** (1). Metallic layers (4,5) are **secured** to opposite sides (2,3) of the board, and on top of these are mounted respective **layers** (10,11) of **elastomeric** material. An electrically-conductive layer (20) is laid on top of the upper **elastomeric layer** (10) and this is formed in a pattern of contact elements (70) and tracks which are interconnected to other layers of the substrate by plated-through holes.

The chip carrier (50) is supported on a heat transfer pad (40) of **copper** which rests on the upper metallic layer (4) and is **secured** to it by a layer of **solder** (46). The pad (40) may have an integral pillar (42) that extends through a **copper**-plated aperture (43) in the substrate to a heat-dissipating pad on the surface of the lower **elastomeric layer.**

ADVANTAGE - **Contact pads** (51) on the chip carrier (50) are **soldered** to the contact elements (70), the height of the heat-transfer pad (40) being such as to separate them and ensure a thick **solder** joint (53).

3/3

Abstract (Equivalent): GB 2135525 B

A leadless chip-carrier substrate arranged to support and provide electrical interconnection with a leadless chip carrier of the kind having a plurality of electrical **contact pads** spaced around its lower edge, including a rigid or semi-rigid multi-layer **circuit board** having a plurality of electrical contact elements on its upper surface, at least one metal heat-dissipating layer and a metal **pad** in thermal **contact** with both the heat-dissipating layer and the lower face of the leadless chip carrier so that heat dissipated by the chip carrier is conducted via the pad to the heat-dissipating layer, wherein the size and thickness of the metal pad is selected such that the edges of the chip carrier overhang the metal pad and such that the

contact pads on the chip carrier are spaced above the contact elements on the **circuit board** thereby increasing the thickness of the **solder** joints between the **contact pads** on the chip carrier and the contact elements on the **circuit board.**

Abstract (Equivalent): US 4509096 A

Layers of **copper**-clad invar are **secured** to opposite sides of a multi-layer **circuit board,** and on top of the **copper** layers are mounted respective **layers** of **elastomeric** material. An electrically-conductive layer is laid on top of the upper **elastomeric layer** and formed in a pattern of contact elements, and tracks which are interconnected to other layers of the substrate by plated holes. The chip carrier is supported on a heat transfer pad of **copper** which rests on the upper invar layer and is **secured** by a layer of **solder.**

Contact pads on the chip carrier are **soldered** to the contact elements, the height of the heat-transfer pad being such as

to separate them and ensure a thick **solder** joint. The **solder** joints and the **solder** under the heat-transfer pad apply a force urging the carrier into close **contact** with the **pad**. **Heat** is **conducted** away from the underside of the carrier by the pad to the top invar layer.

(7pp

44/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015911126
WPI Acc No: 2004-068966/200407
Related WPI Acc No: 2003-862823
XRAM Acc No: C04-028494
XRPX Acc No: N04-055455

Interconnection substrate for use in semiconductor assembly comprises support of electrically insulating material having **contact pads** disposed on surface of support

Patent Assignee: JAMES R D (JAME-I); STARK L E (STAR-I); TEXAS INSTR INC (TEXI)
Inventor: JAMES R D; STARK L E

Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030153160	A1	20030814	US 99152438	P	19990903	200407 B
			US 2000654540	A	20000901	
			US 2003370140	A	20030219	
US 6689678	B2	20040210	US 99152438	P	19990903	200414
			US 2000654540	A	20000901	
			US 2003370140	A	20030219	

Priority Applications (No Type Date): US 99152438 P 19990903; US 2000654540 A 20000901; US 2003370140 A 20030219
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030153160	A1		9	H01L-021/76	Provisional application US 99152438
					Div ex application US 2000654540
					Div ex patent US 6583515
US 6689678	B2			H01L-021/44	Provisional application US 99152438
					Div ex application US 2000654540
					Div ex patent US 6583515

Abstract (Basic): US 20030153160 A1
Abstract (Basic):

NOVELTY - An interconnection substrate comprises support (14) of electrically insulating material having **contact pads** (13) disposed on surface of support. The pads have a composition for **solder attachment** (12).

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for:

(a) a semiconductor assembly comprising substrate having support of electrically insulating material with first and second surface (14a, 14b), electrically conductive routing strips integral with substrate, **contact pads** disposed in pattern on first surface and **connected** to routing strips, **integrated circuit chip** (10) **attached** to second substrate surface, and **solder connections** reflowed into **contact pads**;

(b) a process for fabricating interconnection substrate comprising providing support of electrically insulating material, providing sheet-like elastic **polymer** (17), aligning **polymer** sheet with support, and **attaching polymer** sheet to support surface using **elevated temperature**; and

(c) a process for fabricating semiconductor assembly comprising providing substrate having electrically insulating support, **attaching integrated circuit chip** to second substrate surface, electrically **connecting chip** to second surface using **bonding wires**, surrounding **chip** and

bonding wires with encapsulation compound, positioning one **solder ball** in each openings (18), **elevating** the **temperature** to reflow **solder**, and lowering reflow temperature to room temperature to volumetrically shrink **polymer** more than **solder** to create gap between and opening walls.

USE - For use in semiconductor assembly (claimed) e.g. **ball grid array** (**BGA**).

ADVANTAGE - The method eliminates thermomechanical stress sensitivity of **BGA connections**.

DESCRIPTION OF DRAWING(S) - The figure is a schematic and simplified cross section of **BGA** package having a substrate with a sheet-like **polymer**.

Integrated circuit chip (10)
Solder attachment (12)
Contact pads (13)
Support (14)
First and second surface (14a, 14b)
Sheet-like elastic **polymer** (17)
Openings (18)
pp; 9 DwgNo 1/6

46/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6482541 INSPEC Abstract Number: B2000-03-0170J-029
Title: Solderless interconnection and packaging technique for embedded active components
Author(s): Kujala, A.; Tuominen, R.; Kivilahti, J.K.
Author Affiliation: Lab. of Electron. Production Technol., Helsinki Univ. of Technol., Espoo, Finland
Conference Title: 1999 Proceedings. 49th Electronic Components and Technology Conference (Cat. No.99CH36299) p.155-9
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 1999 Country of Publication: USA xxxii+1289 pp.
ISBN: 0 7803 5231 9 Material Identity Number: XX-1999-02031
U.S. Copyright Clearance Center Code: 0 7803 5231 9/99/$10.00
Conference Title: 1999 Proceedings. 49th Electronic Components and Technology Conference
Conference Date: 1-4 June 1999 Conference Location: San Diego, CA, USA
Language: English
Abstract: In the present study a solderless interconnection and packaging technique for active components is presented. It is based on electroless **copper** deposition directly onto photodefined wiring tracks **connecting** the (I/O) pads of embedded active components. In this manner **better electrical** conductivity, higher reliability and accuracy of ultra fine-pitch interconnections in a low-cost multichip module are achieved. This non-vacuum and solderless **copper/ polymer** process which makes use of a photosensitive epoxy resin, has been used for interconnecting successfully the pads as small as 30*30 mu m/sup 2/. It is emphasized that this solderless process enables the production of reliable electrical **connections** at ambient temperature without difficulties related to mechanical and thermal stability of very small **solder** joints. Detailed microstructural observations of interconnected test **chips** each containing 376 **contact pads** revealed good chemically bonded interfaces. The electrical performance of the embedded active components is also briefly discussed.
Subfile: B

46/3,AB/2 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

16008584 PASCAL No.: 03-0153982
A high performance **polymer** thin film Power electronics packaging technology
IMAPS : international symposium on microelectronics : Denver CO, 4-6 September 2002
FILLION Ray; DELGADO Eladio; MCCONNELEE Paul; BEAUPRE Richard
GE Global Research Center, Niskayuna, NY 12309, United States
International Microelectronics and Packaging Society, United States
International symposium on microelectronics (Denver CO USA) 2002-09-04
Journal: SPIE proceedings series, 2002, 4931 408-414
Language: English
GE Global Research Center has developed a new packaging technology targeted at high performance, high power applications. The technology is called Power Overlay (POL) and involves the use of flex based interconnect structures to package and interconnect power electronic devices. The basic structure has multiple bare **chip** power transistors and/or diodes

solder attached directly down to a thick **copper** metallization on a high **thermal conductivity** substrate. The topside of the power devices are bonded to the bottom of a thin polyimide film **coated** with a **polymeric adhesive**. The **film** contains large via openings (250 microns or larger) and with thick **copper** (100 microns or more) filling the via holes, making a metallurgical **contact** to the **chip pads** and forming a topside interconnect structure. A standard electronics grade encapsulatesis used to fill the gaps between **chips**, providing electrical breakdown protection, moisture protection, mechanical structure and stress relief. This structure has exceptional thermal and electrical performance, a small footprint, a thin profile, and high reliability. The top surface, which is planar, can also be used for heat removal either as an alternative to the backside cooling or as a second thermal path with double sided cooling. POL test results have shown 2x to 3x thermal improvement. The excellent electrical performance is derived from the replacement of wirebonds, with their high electrical parasitics, with a planar interconnect structure with low electrical parasitics. POL modules have demonstrated >80% reductions in overshoot, 3:1 improvements in thermal performance, and 10:1 reduction in inductive and resistive parasitics. POL power modules are capable of hundreds of watts dissipation per square inch, and are designed to handle more than 2000 V and more than 1000 A. The POL process was developed with low cost in mind, with no need for fine line photo-patterning, micro-vias, laser ablation nor precision Pick & Place equipment. This paper provides details of the POL process and structures, shows working modules and presents performance and reliability data.

46/3,AB/3 (Item 2 from file: 144)
DIALOG(R)File 144:Pascal

16003446 PASCAL No.: 03-0148810

Current-carrying capacity of anisotropic-conductive film joints for the flip **chip** on flex applications

FAN S H; CHAN Y C

Department of Electronic Engineering, City University of Hong Kong, Kowloon, Hong Kong

Journal: Journal of electronic materials, 2003, 32 (2) 101-108

Language: English

The effect of the substrate-pad physical properties (surface roughness and hardness) on the current-carrying capacity of anisotropic-conductive film (ACF) joints is investigated in this work. Flip **chips** with Au bumps were bonded to the flexible substrates with Au/**Cu** and Au/Ni/**Cu** pads using different bonding pressure. It was found that the current-carrying capacity of ACF joints increased to a maximum value with the rise of the bonding pressure; then, it reduced if the bonding pressure continually increased. The maximum average value per unit area of Au/Ni/**Cu** pad and Au/**Cu** pad ACF joints is about 93 mu A/ mu m SUP 2 and 118 mu A/ mu m SUP 2 , respectively, at 100-MPa bonding pressure. The variation trend of **connection** resistance is the opposite of current-carrying capacity. The variation of current-carrying capacity (or **connection** resistance) of Au/**Cu** pad joints is larger than that of Au/Ni/**Cu** pad joints. The current-carrying capacity is related to the variation of the resistance of ACF joints. The **connection** resistance of ACF joints depends primarily on the particle constriction resistance (R SUB c SUB o SUB i), R SUB c SUB o SUB i alpha 1/a, where "a" is the radius of contact spot. A smaller contact area results in larger joule heat generation per unit volume (Qg), Qg 1/a SUP 4 , which

preferentially **elevates** the **temperature** of the constriction. The **raised temperature increases** the resistance because of the temperature-dependent coefficient of the metal resistivity. The theory of tribology is used to explain the difference between Au/**Cu** pad and Au/Ni/**Cu** pad ACF joints. For the Au/**Cu** pad ACF joints, the deformation of the particles' upper and bottom sides is nearly symmetrical; the contact between conductive particles and pad has the character of "sliding contact," especially under high pressure. For the Au/Ni/**Cu pad** ACF joint, the **contact** between particles and **pad** determined the conduction characteristics of ACF joints. It has the character of "static contact." Thus, the current-carrying capacity (or **connection** resistance) ofAu/**Cu** pad joints is more sensitive to the bonding pressure.

46/3,AB/4 (Item 3 from file: 144)
DIALOG(R)File 144:Pascal

15322695 PASCAL No.: 02-0008427
Laser **soldering** for **chip**-on-glass mounting in flat panel display application
Special Issue on Lead-Free **Solder** Materials and **Soldering** Technologies
LEE Jong-Hyun; KIM Won-Yong; AHN Dong-Hoon; LEE Yong-Ho; KIM Yong-Seog
KANG Sung K, ed; MAVOORI Hareesh, ed; CHADA Srinivas, ed; KAO C Robert, ed; SMITH Ronald W, ed
Hong Ik University, Department of Metallurgy and Materials Science, Seoul , Korea, Republic of; Meccatechs Co. Ltd., Yonginsi, Kyungkido, Korea, Republic of
IBM T.J. Watson Research Center, Yorktown Heights, NY 10598, United States; Lucent Technologies/Agere Systems, Bell Laboratories, 700 Mountain Avenue, Murray Hill, NJ 07974, United States; Motorola, 8000 West Sunrise Boulevard, Fort Lauderdale, FL 33322, United States; National Central University, Department of Chemical & Materials Engineering, Chungli City, Taiwan; Materials Resources International, 403 Elm Avenue, North Wales, PA 19454, United States
Minerals, Metals & Materials Society (TMS). Electronic, Magnetic & Photonic Materials Division. Electronic Packaging and Interconnections Materials Committee, Warrendale, PA 15086, United States
Symposium on Lead-Free Solder Materials and Soldering Technologies (New Orleans, Louisiana USA) 2001-02
Journal: Journal of electronic materials, 2001, 30 (9) 1255-1261
Language: English
Chip -on-glass (COG) mounting of area array electronic packages was attempted by heating the rear surface of a **contact pad** film deposited on a glass substrate. The pads consisted of an adhesion (i.e., Cr or Ti) and a top coating layer (i.e., Ni or **Cu**) was heated by an UV laser beam transmitted through the glass substrate. The laser energy absorbed on the pad **raised** the **temperature** of a **solder ball** which was in physical **contact** with the **pad**, forming a reflowed **solder bump** . The effects of the adhesion and top coating layer on the laser reflow **soldering** were studied by measuring the temperature profile of the ball during the laser heating process. The results were discussed based on the measurement of reflectivity of the adhesion layer. In addition, the microstructures of **solder bumps** and their mechanical properties were examined.

46/3,AB/5 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015703727
WPI Acc No: 2003-765920/200372
Related WPI Acc No: 2003-110417; 2003-416923
XRAM Acc No: C03-210374
XRPX Acc No: N03-613474
Multilayer interconnect structure for electronic package comprises liquid crystal dielectric layer directly bonded to surfaces of **thermally conductive** layer and electroconductive layer within each dielectric layer
Patent Assignee: IBM CORP (IBMC); INT BUSINESS MACHINES CORP (IBMC)
Inventor: EGITTO F D; FARQUHAR D S; MARKOVICH V R; POLIKS M D; POWELL D O
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030147227	A1	20030807	US 200267551	A	20020205	200372 B
			US 2002263849	A	20021003	
JP 2004128497	A	20040422	JP 2003334361	A	20030925	200428

Priority Applications (No Type Date): US 2002263849 A 20021003; US 200267551 A 20020205
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030147227	A1		25	H05K-001/11	CIP of application US 200267551
JP 2004128497	A		44	H01L-023/12	

Abstract (Basic): US 20030147227 A1
Abstract (Basic):
NOVELTY - A multiply interconnect structure (18) comprises:
(a) a liquid crystal **polymer** (LCP) dielectric layer (38, 34) directly bonded to each opposing surface (24, 26) of a **thermally conductive** layer (22) with no extrinsic **adhesive** material bonding the LCP dielectric layer to the **thermally conductive** layer; and
(b) an electroconductive layer within each LCP dielectric layer
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for:
(a) a method of making a multiply interconnect structure by providing a **thermally conductive** layer including first and second opposing surfaces; positioning a first LCP dielectric layer on the first opposing surface of the **thermally conductive** layer; positioning a second LCP dielectric layer on the second opposing surface of the **thermally conductive** layer; and subjecting the first and second LCP dielectric layers to a first and second temperature that are less than the nematic-to-isotropic transition temperature of the respective LCP dielectric materials for a dwell time and at an elevated pressure that is sufficient to cause the first and second LCP dielectric materials to plastically deform and to cause bonding of the first LCP dielectric sublayer to the **thermally conductive layer** without any extrinsic **adhesive layer** disposed between the first LCP dielectric sublayer and the **thermally conductive** layer and bonding of the second LCP dielectric layer to the **thermally conductive layer** without any extrinsic **adhesive layer** disposed between the second LCP dielectric sublayer and the **thermally conductive**

layer;

(b) an electrical structure comprising a first 2S1P sub-structure comprising a first dielectric layer, a first power plane within the first dielectric layer, a top signal plane on a top surface of the first dielectric layer, a bottom signal plane on a bottom surface of the first dielectric layer, and a first electrically conductive via; a second 2S1P sub-structure comprising a second dielectric layer, a second power plane within the second dielectric layer, a top signal plane on a top surface of the second dielectric layer, a bottom signal plane on a bottom surface of the second dielectric layer, and a second electrically conductive via; and a joining layer having first and second opposing surfaces and an electrically conductive plug and comprising LCP dielectric material, wherein the first opposing surface is directly bonded to the first dielectric layer of the first 2S1P sub-structure, the second opposing surface is directly bonded to the second dielectric layer of the second 2S1P sub-structure and the electrically conductive plug electrically couples the first electrically conductive via to the second electrically conductive via; and

(c) a method for forming an electrical structure by providing a first 2S1P sub-structure; providing a second 2S1P sub-structure; providing a joining layer; and directly bonding the joining layer to the first dielectric layer of the first 2S1P sub-structure at the first opposing surface and to the second dielectric layer of the second 2S1P sub-structure at the second opposing surface.

USE - Electronic package.

ADVANTAGE - Reduces processing time and processing costs and reduces dielectric layer thickness in the fabrication of organic substrates. The LCP dielectric layer can be purchased in a **copper** clad format. This eliminates the need for a first step of laminating **copper** foil to a dielectric layer. The LCP dielectric layer is more stable and tear-resistant than a Rogers 2800 dielectric material or a partially cured thermoset material. It can be handled in thinner sheets. This avoids the use of extra thick **copper** for a central power plane so that there is enhancement of subtractive circuitization and subsequent filling of fine features.

DESCRIPTION OF DRAWING(S) - The figure shows a front section of an electronic package that includes a semiconductor **chip** assembled to a multilayered interconnect structure assembled to a circuitized substrate.

Semiconductor **chip** (12)
Contacts (16)
Multilayered interconnect structure (18)
Thermally conductive layer (22)
First and second opposing surfaces (24, 26)
First LCP dielectric layer (28)
First dielectric sublayers (29, 30-32, 39)
Second LCP dielectric layer (34)
Second dielectric sublayers (35-38, 41)
Electrically conductive components (40, 42)
Electrically conductive material (45)
Third dielectric layer (46)
Solder connections (47)
Plated through hole (50, 52)
Circuitized substrate (100)
Contact pads (103)
pp; 25 DwgNo 1/25

46/3,AB/6 (Item 2 from file: 350)

015615975
WPI Acc No: 2003-678132/200364
Related WPI Acc No: 2002-636107
XRAM Acc No: C03-185174
XRPX Acc No: N03-541371

Bumping process for **chip** scale packaging, involves forming under bump metal structure and then leaded bump on each bonding pad, forming thermosetting plastic on **chip**'s active surface, and grinding surface of the plastic

Patent Assignee: FANG J (FANG-I)
Inventor: FANG J

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030099767	A1	20030529	US 2001815804	A	20010323	200364 B
			US 2002329265	A	20021224	

Priority Applications (No Type Date): TW 2001101426 A 20010120
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030099767	A1		12	B05D-005/12	Div ex application US 2001815804

Abstract (Basic): US 20030099767 A1
Abstract (Basic):

NOVELTY - A bumping process for **chip** scale packaging comprises forming sequentially an under bump metal structure and a leaded bump respectively on each bonding pad of a **chip**; forming a thermosetting plastic on an active surface of the **chip** to cover the leaded bumps; and grinding the surface of the thermosetting plastic to expose the leaded bumps.

DETAILED DESCRIPTION - A bumping process for **chip** scale packaging comprises:

(a) providing a **chip** (202) having an active surface (202a) with bonding pads (206);

(b) forming a passivation layer (203) on the active surface exposing the bonding pads;

(c) forming an under bump metal (UBM) structure (208) on each bonding pad;

(d) forming leaded bumps (210) respectively on the UBM structures;

(e) forming a thermosetting plastic (212) on the active surface that covers the leaded bumps; and

(f) grinding the surface of the thermosetting plastic to expose the leaded bumps.

The material of the leaded bumps comprises tin and lead. The lead constituent is above 85%.

USE - For **chip** scale packaging.

ADVANTAGE - The inventive process can eliminate the need for an underfill process, overcomes the related **high degree** of difficulty in workability, and can increase production throughput.

DESCRIPTION OF DRAWING(S) - The figure is a schematic view of a bumping process for **chip** scale packaging.

Chip (202)
Active surface (202a)
Passivation layer (203)
Bonding pads (206)
UBM structure (208)
Leaded bumps (210)

Thermosetting plastic (212)
Carrier (260)
Contact pads (262)
Solder paste (264)
pp; 12 DwgNo 9/19

46/3,AB/7 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015583471
WPI Acc No: 2003-645628/200361
Related WPI Acc No: 2003-829531
XRAM Acc No: C03-176461
XRPX Acc No: N03-513670
Cylindrical bonding structure, for use in **connecting chip** substrate to form flip-**chip** package, comprises conductive cylinder on bonding pad of **chip** and **solder** block on conductive cylinder
Patent Assignee: CHOU C (CHOU-I); KUO H (KUOH-I); LEE J (LEEJ-I); LIN S (LINS-I)
Inventor: CHOU C; KUO H; LEE J; LIN S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030129822	A1	20030710	US 200255580	A	20020122	200361 B
			US 2002174357	A	20020617	

Priority Applications (No Type Date): TW 2002100092 A 20020107
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030129822	A1		20	H01L-021/44	Div ex application US 200255580

Abstract (Basic): US 20030129822 A1
Abstract (Basic):
NOVELTY - A cylindrical bonding structure (360) comprises conductive cylinder (340) on bonding pad (314) of **chip** (316) and **solder** block on conductive cylinder
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for:
(a) a method of forming cylindrical bonding structures over silicon **wafer** comprising forming ball contact metallic layer (320) over the entire active surface of the silicon **wafer** including bonding pads, forming patterned mask layer over the ball contact metallic layer, depositing conductive material into the opening to form conductive cylinder over the ball contact metallic layer, depositing **solder** material into the remaining space of the opening to form cylindrical **solder** cap on the upper surface of the conductive cylinder, and removing the mask layer and the ball contact metallic layer outside the conductive cylinder; and
(b) a method of **connecting** a **chip** to substrate to form flip-**chip** package comprising forming cylindrical bonding structure on the bonding pad of the **chip**, flipping over the active surface of the **chip** to face the substrate surface so that upper surface of the **solder** block **contacts** the junction **pad**, and **conducting** reflow process to **melt** the **solder** block material so that the conductive cylinder and the junction pad are joined together.
USE - Used in **connecting chip** substrate to form flip-**chip** package (claimed).

ADVANTAGE - The process is capable of reducing the separation between neighboring bonding pads on **chip** while increasing distance of separation between the **chip** and substrate. The post-packaging life of the **chip** is extended. IT enables the production cost of flip-**chip** package to be reduced.

DESCRIPTION OF DRAWING(S) - The figure is a cross-section of a cylindrical bonding structure during production.

Bonding pad (314)

Chip (316)

Ball contact metallic layer (320)

Conductive cylinder (340)

Solder ball (350)

Cylindrical bonding structure (360)

pp; 20 DwgNo 3E/6

46/3,AB/8 (Item 4 from file: 350)

DIALOG(R)File 350:Derwent WPIX

015088373

WPI Acc No: 2003-148891/200314

Related WPI Acc No: 2002-382395; 2002-479530; 2002-507386; 2003-200698

XRAM Acc No: C03-038675

XRPX Acc No: N03-117494

Enhancing electrical contact surface(s), e.g. **contact pad**, by co-depositing first metal layer and particle(s) on the surface by electroless deposition, activating the particle(s) and depositing second metal layer

Patent Assignee: NANOPIERCE TECHNOLOGIES INC (NANO-N)

Inventor: BAHN R J; BLUM F A; NEUHAUS H J; ZOU B

Number of Countries: 099 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 2002102524	A1	20021227	WO 2002US18214	A	20020607	200314	B

Priority Applications (No Type Date): US 2001883012 A 20010615

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 2002102524	A1	E	29	B05D-005/12	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VN YU ZA ZM ZW

Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZM ZW

Abstract (Basic): WO 2002102524 A1

Abstract (Basic):

NOVELTY - Electrical contact surface(s) is improved to provide an improved electrical, thermal and/or mechanical **connection** with opposing electrical contact surface(s) by co-depositing a first layer of a first meta and particle(s) on the electrical contact surface(s) by electroless deposition. The particle(s) is then activated before a second layer of second metal is deposited.

DETAILED DESCRIPTION - Improving electrical contact surface(s) to provide an improved electrical, thermal and/or mechanical **connection** with opposing electrical contact surface(s) involves co-depositing a first layer of first metal (102) and particle(s) (104)

on the electrical contact surface(s) by electroless deposition. The particle(s) is trapped by the deposition of the first metal on the electrical contact surface. The particle(s) is then activated to accept subsequent deposition of a second layer of metal (106).

USE - Used for improving electrical contact surface(s) to provide an improved electrical, thermal and/or mechanical **connection** with at least one opposing electrical contact surface (claimed).

ADVANTAGE - The process is able to uniformly deposit metal and particles of any shape, and with a wide range of density and sizes on contact surfaces. It can be adjusted to provide any desired surface area coverage in desirable deposition patterns. The co-deposited contact surface can be easily joined to another surface of any type by non-conductive **adhesive** resulting in a **connection** that is mechanically robust, chemically inert and inherently electrically conductive. This eliminates the necessity of using specialized **conductive adhesive** or extreme **heat** for **soldering** or bump reflow for creating electrical surface joints.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-section of the contact surface with the addition of second metal plated layer.

Electrical contact surface (100)
First metal layer (102)
Second metal layer (106)
pp; 29 DwgNo 1C/7

46/3,AB/9 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014300242
WPI Acc No: 2002-120946/200216
Related WPI Acc No: 2001-069604
XRAM Acc No: C02-036897
XRPX Acc No: N02-090698
Making of socketable **ball grid array** assembly, by applying **adhesive** onto terminal pads of **chip** carrier module, bonding spheres to terminal pads, and plugging array of spheres into sockets in printed wiring board
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: CALL A J; DELAURENTIS S A; FAROOQ S; KANG S K; PURUSHOTHAMAN S; STALTER K A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6300164	B1	20011009	US 9752094	P	19970710	200216	B
			US 98106779	A	19980630		
			US 2000559314	A	20000427		

Priority Applications (No Type Date): US 9752094 P 19970710; US 98106779 A 19980630; US 2000559314 A 20000427
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6300164	B1		8	H01L-021/44	Provisional application US 9752094 Div ex application US 98106779

Abstract (Basic): US 6300164 B1
Abstract (Basic):
NOVELTY - A socketable **ball grid array** (**BGA**) assembly is made by applying an electrically conducting **adhesive** onto terminal pads of a **chip** carrier module,

bonding conducting spheres to the terminal pads through the conducting **adhesive**, and plugging the array of spheres into sockets in a printed wiring board.

DETAILED DESCRIPTION - Making of a socketable **BGA** assembly, involves a) applying an electrically conducting **adhesive** (34) including a thermoplastic or thermosetting resin matrix, no clean **solder** flux, and electrically conducting particles with an electrically conductive and fusible coating with at least some of the particles being fused to the other particles through the fusible coating, onto terminal pads (33) of a **chip** carrier (32) module; b) aligning and placing the module on an array of conducting spheres (36) in a carrier boat; c) bonding the spheres to the terminal pads through the **conducting adhesive** by applying **heat** and pressure to allow melting of the fusible coating and bonding of the particles to themselves, to the terminal pads and to the spheres as well as curing of the **polymer** resin to form a strong joint; d) optionally cleaning the unjoined area of the spheres to remove any residues; and e) plugging the array of spheres into sockets in a printed wiring board (40).

USE - For making a socketable **BGA** assembly.

ADVANTAGE - The invention provides a socketable **BGA** assembly that can be readily demounted from the printed wiring board they are assembled onto.

DESCRIPTION OF DRAWING(S) - The figure is a schematic cross-sectional illustration representing a new **solder ball connection** scheme in a ceramic **BGA**, where a stiff and electrically conductive ball is **connected** to the module.

Chip carrier (32)
Terminal pads (33)
Electrically conducting **adhesive** (34)
Printed wiring board (40)
pp; 8 DwgNo 3/3

46/3,AB/10 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013469661
WPI Acc No: 2000-641604/200062
XRPX Acc No: N00-475853
Connection material has low **melting** point **conductor** layers formed on either sides of high **melting** point **conductor** core
Patent Assignee: SHINKO DENKI KOGYO KK (SHIA)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2000232119	A	20000822	JP 9932211	A	19990210	200062	B

Priority Applications (No Type Date): JP 9932211 A 19990210
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2000232119	A		9	H01L-021/60	

Abstract (Basic): JP 2000232119 A
Abstract (Basic):

NOVELTY - Conductor layer (110) made of low-melting point material is formed on either sides of conductor core (100) made of refractory material like **copper** or high melting point **solder**.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) manufacturing method of semiconductor **chip**;

(b) **connection** procedure of semiconductor **chip**

USE - For **connecting electrode** of semiconductor **chip** and **contact pads** of wiring board.

ADVANTAGE - Since **conductor** layer having low-**melting** point is formed on laminated **conductor** core having high-**melting** point, **electrodes** of semiconductor **chip** and **contact pads** of wiring board can be **connected** easily and quickly with soft **soldering**.

DESCRIPTION OF DRAWING(S) - The figure shows perspective diagram of **connection** material.

Conductor core (100)

Conductor layer (110)

pp; 9 DwgNo 1/16

46/3,AB/11 (Item 7 from file: 350)

DIALOG(R)File 350:Derwent WPIX

007550588

WPI Acc No: 1988-184520/198827

XRPX Acc No: N88-140979

Integrated circuit chip packaging construction - has insulating frames sandwiched between **thermally conductive** covers and low-resistance leads passing through frames

Patent Assignee: TRW INC (THOP)

Inventor: SMOLLEY R

Number of Countries: 009 Number of Patents: 004

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 273556	A	19880706	EP 87309841	A	19871106	198827	B
JP 63174339	A	19880718	JP 87320058	A	19871217	198834	
PH 26354	A	19920429	PH 36234	A	19871215	199601	
KR 9603765	B1	19960322	KR 8714598	A	19871221	199912	

Priority Applications (No Type Date): US 86944124 A 19861222

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 273556	A	E	7		
	Designated States (Regional): DE FR GB IT NL SE				
PH 26354	A			H01L-021/58	
KR 9603765	B1			H01L-023/06	

Abstract (Basic): EP 273556 A

The upper and lower covers (14,12) are made of **copper** or of an aluminium-beryllium alloy and have high **thermal conductivity**, high corrosion resistance and are malleable. A pair of insulating frames (18,20) act for **sealing** hermetically the **IC chip** (16) in the **chip** package. Low-resistance input-output leads extend through openings in the insulating frames and **connect** with the **chip** by five wires **soldered** to the leads and to **contact pads** on the **IC chip**. The insulating frames are made of a glass ceramic material having a coefficient of expansion which matches that of the upper and lower covers.

ADVANTAGE - Covers **conduct heat** from **IC chip** and reduce operating temp. package can be assembled at

relatively low temps. allowing use of **copper** input-output leads having relatively low melting point and low electrical resistance.

1/4

```
? DS40-

Set     Items   Description
S40         4   RD (unique items)
S41        17   S37 NOT S39
S42        13   S41 AND S24
S43        12   RD (unique items)
S44         1   S43 AND S27
S45        11   S43 NOT S44
S46        11   RD (unique items)
? S S41 NOT S42
              17  S41
              13  S42
     S47       4  S41 NOT S42
? RD
>>>Duplicate detection is not supported for File 350.
>>>Duplicate detection is not supported for File 347.
>>>Duplicate detection is not supported for File 344.
>>>Duplicate detection is not supported for File 371.

>>>Records from unsupported files will be retained in the RD set.
...completed examining records
     S48       4  RD (unique items)
? TA
>>>No matching display code(s) found in file(s): 65

 48/3,AB/1     (Item 1 from file: 2)
DIALOG(R)File   2:INSPEC
(c) 2004 Institution of Electrical Engineers. All rts. reserv.

03080591   INSPEC Abstract Number: A88039863, B88020258
  Title: Method for making low-resistivity contacts to high T/sub c/
superconductors
  Author(s): Ekin, J.W.; Panson, A.J.; Blankenship, B.A.
  Author  Affiliation: Electromagnetic Technol. Div., NBS, Boulder, CO, USA

  Journal: Applied Physics Letters    vol.52, no.4    p.331-3
  Publication Date: 25 Jan. 1988  Country of Publication: USA
  CODEN: APPLAB  ISSN: 0003-6951
  U.S. Copyright Clearance Center Code: 0003-6951/88/040331-03$01.00
  Language: English
```

Abstract: A method for making low-resistivity contacts to high T/sub c/ superconductors has been developed, which has achieved contact surface resistivities less than 10 mu Omega cm/sup 2/ at 76 K and does not require sample heating above approximately 150 degrees C. This is an upper limit for the contact resistivity obtained at high current densities up to 10/sup 2/-10/sup 3/ A/cm/sup 2/ across the contact interface. At lower measuring current densities the contact resistivities were lower and the voltage-current curve was nonlinear, having a superconducting transition character. On cooling from 295 to 76 K, the contact resistivity decreased several times, in contrast to indium **solder** contacts where the resistivity increased on cooling. The contacts showed consistently low resistivity and little degradation when exposed to dry air over a four-month period and when repeatedly cycled between room temperature and 76 K. The contacts are formed by sputter depositing a layer of a noble metal-silver and gold were used-on a clean superconductor surface to protect the surface and serve as a **contact pad.** External

connections to the **contact pads** have been made using both **solder** and wire-bonding techniques.
Subfile: A B

48/3,AB/2 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS

1385366 NTIS Accession Number: PB88-228283
Effect of Oxygen Annealing on Low-Resistivity Contacts for High-T (sub c) Superconductors
(Final rept)
Ekin, J. W. ; Panson, A. J. ; Blankenship, B. A.
National Bureau of Standards (NEL), Boulder, CO. Electromagnetic Technology Div.
Corp. Source Codes: 076364003
Sponsor: Department of Energy, Washington, DC.
1988 4p
Languages: English Document Type: Journal article
Journal Announcement: GRAI8820
Sponsored by Department of Energy, Washington, DC.
Pub. in Materials Research Society Symposia Proceedings, v99 p283-286 1988.
NTIS Prices: Not available NTIS
A method for making low resistivity contacts to high-Tc superconductors has been developed, consisting of depositing noble metal **contact pads** (silver or gold) on a clean superconductor surface at low temperatures (<150 deg C). After annealing the silver **contact pads** in oxygen at intermediate temperatures (= or < 500 C) for one hour, contact resistivities less than 2 x 10 to the -8th power ohm-cm sq at 76 K are obtained, about six orders of magnitude less than for indium-**solder** contacts. Before annealing, the contact resistivities are still very low, in the 10 to the -6th to 10 to the -5th ohm-cm sq range at 76 K, which would be useful when contacts with low fabrication temperatures are required. The voltage-current characteristics of the contacts are strongly nonlinear after annealing, having a superconducting transition character. This is ascribed to the critical current of the superconducting material being exceeded at the contact interface. External **connections** to the **contact pads** have been made using both **solder** and thermosonic wire-bonding techniques.

48/3,AB/3 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013065149
WPI Acc No: 2000-237021/200020
Related WPI Acc No: 1999-061825; 1999-142234
XRAM Acc No: C00-072073
XRPX Acc No: N00-177751
Adhesively and **solder bonded** capacitive filter feed-through for implantable medical devices
Patent Assignee: MEDTRONIC INC (MEDT)
Inventor: FRALEY M A; HOCH R F; SEIFRIED L M; WOLF W D
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6031710	A	20000229	US 97852198	A	19970506	200020	B

Priority Applications (No Type Date): US 97993974 A 19971218; US 97852198 A 19970506
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6031710	A		20	H01G-004/35	CIP of application US 97852198 CIP of patent US 5870272

Abstract (Basic): US 6031710 A
Abstract (Basic):

NOVELTY - The feed-through assembly consists of an electroconductive ferrule within the aperture of an insulator, an electroconductive pin extending into the aperture of the insulator, an electroconductive inner **braze** joint at the top of the pin or between the pin and the aperture sidewalls, and an electroconductive intermediate **braze** joint between the insulator and sidewalls of the aperture of the ferrule. A ceramic-containing capacitive filter has an electroconductive inner **adhesive** or **solder** joints within its aperture **connected** to the inner **braze** joint and its first terminal. An electroconductive outer **adhesive** or **solder** joint is formed between the ferrule and **connected** to the filter's second terminal.

DETAILED DESCRIPTION - The feed-through assembly consists of an electroconductive ferrule within the aperture of an insulator, and an electroconductive pin extending into the aperture of the insulator. The ferrule and pin are made of at least one of titanium, niobium, platinum, molybdenum, zirconium, tantalum, vanadium, tungsten, iridium, rhodium, rhenium, osmium, ruthenium, palladium, silver or their alloys. An electroconductive inner **braze** joint at the top of the pin or between the pin and the aperture sidewalls, and an electroconductive intermediate **braze** joint between the insulator and sidewalls of the aperture of the ferrule are formed of one or more of (1) pure gold, (2) a gold alloy containing at least one of titanium, niobium, vanadium, nickel, platinum, molybdenum, palladium, ruthenium, silver, iridium, rhodium, osmium or their alloys, (3) a **copper** silver alloy optionally containing at least one of iridium, titanium, tin, gallium, palladium or platinum, and (4) a silver palladium gallium alloy. A ceramic-containing capacitive filter has an electroconductive inner **adhesive** or **solder** joint within its aperture **connected** to the inner **braze** joint and its first terminal. An electroconductive outer **adhesive** or **solder** joint is formed between the ferrule and **connected** to the filter's second terminal. The **solder** is (1) an indium-lead alloy, (2) indium, (3) lead, (4) silver, (5) tin, (6) indium-tin alloy, (7) indium silver alloy, (8) tin lead alloy, (9) tin silver alloy, (10) indium lead silver alloy, (11) tin lead silver alloy, (12) gold tin alloy, (13) gold silicon alloy, (14) gold germanium alloy or (15) gold indium alloy.

USE - The filter attenuates electromagnetic interference when installed within an implantable medical device, including a pacemaker, implantable pulse generator, defibrillator, pacemaker-cardioverter-defibrillator, neurological stimulator or gastrointestinal stimulator (all claimed).

ADVANTAGE - Improved EMI filtering capability. Secondary manufacturing steps such as epoxy application or additional **soldering** is avoided, thus reducing the cost of the device and the cost of implantable medical devices. There is additional mechanical support for the filter. Sputtered capacitors can be used. Low **temperature** solders with **increased** ductility and enhanced

corrosion resistance can be used.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross sectional view of the unipolar feedthrough assembly.

Ferrule (10)
Shield (20)
Conductive pin (30)
Capacitive filter (50)
Inner **adhesive** joint (55)
Inner **braze** joint (65)
pp; 20 DwgNo 1/9

48/3,AB/4 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007549872
WPI Acc No: 1988-183804/198827
XRPX Acc No: N88-140422
Semiconductor hybrid module with components mounted on base plates - forming removable subassemblies enclosed by removable housing
Patent Assignee: SEMIKRON ELEKTRONIK GMBH (SEMK)
Inventor: HEILBRONNER H; SCHIERZ W
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 3643288	A	19880630	DE 3643288	A	19861218	198827	B
JP 63240056	A	19881005	JP 87319094	A	19871218	198846	
DE 3643288	C2	19930422	DE 3643288	A	19861218	199316	

Priority Applications (No Type Date): DE 3643288 A 19861218
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 3643288	A		11		
DE 3643288	C2		7	H01L-025/16	

Abstract (Basic): DE 3643288 A

Each semiconductor element (1), with **connecting** links (2), is **soldered** by one of its contacts to an insulated and **heat conducting** base plate made of oxide ceramic (3) covered with **copper**. The base plate is provided with metal contact layers (32,33) and insulating layers (31) that allow additional components to be **soldered**. the assembly is enclosed in a insulated housing (5).

Both the housing and component assembly are removable from the base (9) to which they are **attached** by means of bolts (4,7,8) to which contact links may be **attached.** The assembly may include active, as well as passive semiconductor components.

USE/ADVANTAGE - Compact assembly, suitable for close integration and with good thermal characteristics, and enabling all components to be tested before assembly.

1/7

Abstract (Equivalent): DE 3643288 C

The electronic module has a solid state element (1) fixed to a disc of insulating material (3) by **soldering** leads to **contact pads** (11) and to power supply terminals (4) formed on a metal coated surface. The base disc can be of oxide ceramic (31) with contact metal on both surfaces (32,33). The unit is located within a housing (5) **secured** to a carrier body (9) by screws. A **connection** to the housing is made using a bridging strip (6) to the terminal

block. Other versions use a spring clip to provide a plate contact. ADVANTAGE - Provides simple means of exchanging modules. (Dwg.1/7)

53/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

016251498
WPI Acc No: 2004-409392/200438
Related WPI Acc No: 2003-755989
XRPX Acc No: N04-325004
Ball grid array package has **bonding wire** whose one is **connected** to **contact pad** on semiconductor **chip** and other end is extended into groove with conductive contacts on top surface of substrate
Patent Assignee: ORIENT SEMICONDUCTOR ELECTRONICS LTD (ORIE-N)
Inventor: CHOU S; LIANG S; YANG C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20040075166	A1	20040422	US 2002196940	A	20020718	200438 B
			US 2003683911	A	20031010	

Priority Applications (No Type Date): US 2003683911 A 20031010; US 2002196940 A 20020718
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20040075166	A1		8	H01L-023/10	CIP of application US 2002196940

Abstract (Basic): US 20040075166 A1
Abstract (Basic):
NOVELTY - An outer frame casing (521) of heat dissipating frame (52), mounted on top surface of dielectric substrate (51) surrounds inner seat casing (522). The interconnecting portions **heat-conductively** interconnect the inner seat and outer frame casings. One end of **bonding wire** (54) is **connected** to **contact pad** on semiconductor **chip** and other end is extended into groove with conductive contacts on top surface of substrate.
USE - **Ball grid array** (**BGA**) package.
ADVANTAGE - The heat generated by semiconductor **chip** can be rapidly and effectively conducted to outer frame casing through inner seat casing and interconnection portions, and thus avoid restriction of number and locations of the conductive contacts on bottom surface of the dielectric substrate.
DESCRIPTION OF DRAWING(S) - The figure shows a sectional view of the **ball grid array** package.
dielectric substrate (51)
heat dissipating frame (52)
bonding wires (54)
outer frame casing (521)
inner seat casing (522)
pp; 8 DwgNo 5/7

53/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015671381
WPI Acc No: 2003-733568/200370
XRPX Acc No: N03-586490

Low-voltage drop **thermally enhanced integrated circuit** package e.g. **ball grid array** package uses heat sink assembly **attached** to **integrated circuit die** and **contact pads** on substrate for both **heat** and signal **conduction**

Patent Assignee: BROADCOM CORP (BROA-N); RAHMAN KHAN R (KHAN-I); ZHONG C H (ZHON-I)

Inventor: KHAN R R; ZHONG C; RAHMAN KHAN R; ZHONG C H

Number of Countries: 032 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 1347513	A2	20030924	EP 20036574	A	20030324	200370 B
US 20030179549	A1	20030925	US 2002366241	P	20020322	200370
			US 2002253600	A	20020925	

Priority Applications (No Type Date): US 2002253600 A 20020925; US 2002366241 P 20020322

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1347513	A2	E	53	H01L-023/433	
	Designated States (Regional): AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LI LT LU LV MC MK NL PT RO SE SI SK TR				
US 20030179549	A1			H05K-007/20	Provisional application US 2002366241

Abstract (Basic): EP 1347513 A2

Abstract (Basic):

NOVELTY - An **integrated circuit** (**IC**) package (700) includes a heat sink assembly (702) comprising heat sink elements (704,706) **attached** to an **IC die** (304) and **contact pads** (720) on a substrate (302) respectively, for **heat** and signal **conduction**.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for **IC** package assembly method.

USE - E.g. land grid array (LGA) package, pin grid array (PGA) package, **chip** scale package (CSP), **ball grid array** (**BGA**) package, quad flat package (QFP) and other **IC** package used in application specific **integrated circuit** (ASIC), microprocessors.

ADVANTAGE - The heat sink is used for both **heat** and signal **conduction**. Hence **wire bond** length is reduced to reduce inductance and resistance. The heat sink with bumps allows direct contact of the **IC die** core with other heat sink element which reduces the voltage drop. The ground or power ring can be formed in the heat sink, hence **chip** area can be used for additional components and effective routing of signals.

DESCRIPTION OF DRAWING(S) - The figure shows a cross- sectional view of the **BGA** package.

substrate (302)
IC die (304)
IC package (700)
heat sink assembly (702)
heat sink elements (704,706)
contact pad (720)
pp; 53 DwgNo 7A/15

53/3,AB/3 (Item 3 from file: 350)

DIALOG(R)File 350:Derwent WPIX

015558037
WPI Acc No: 2003-620193/200359
Related WPI Acc No: 2002-635363; 2002-635365; 2003-420004; 2003-678809; 2003-678811; 2003-678812; 2003-720751; 2004-080035; 2004-080038; 2004-080065; 2004-080066; 2004-256081; 2004-256082
XRPX Acc No: N03-494107
Ball grid array assembling method, involves **connecting wire bond** from **bond** pad of **integrated circuit die** to **contact pad** on substrate through opening in stiffener
Patent Assignee: BROADCOM CORP (BROA-N)
Inventor: KHAN R R; ZHAO S Z
Number of Countries: 031 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1333490	A2	20030806	EP 20031957	A	20030130	200359	B

Priority Applications (No Type Date): US 2002284340 A 20021031; US 2002352877 P 20020201
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1333490	A2	E	79	H01L-023/36	

Designated States (Regional): AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LI LT LU LV MC MK NL PT RO SE SI SK TR

Abstract (Basic): EP 1333490 A2
Abstract (Basic):
NOVELTY - The method involves mounting an **integrated circuit** (**IC**) **die** (102) in a centrally located cavity of a planar top surface of a stiffener (112) and **attaching** the bottom surface of the stiffener to the top surface of a substrate (104). A **wire bond** (108) from a bond pad (118) of the **IC die** is **connected** to a **contact pad** (120) on the substrate through a yore opening (114) in the stiffener.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(1) stiffener for stiffening a substrate in **ball grid array** package;
(2) **ball grid array** package; and
(3) stiffener forming method.
USE - For assembling **IC** package e.g. **ball grid array** (**BGA**) package (claimed).
ADVANTAGE - Improves electrical performance and **heat spreading** property of the **BGA** package. Facilitates **attachment** of electronic devices to the bottom surface of the **BGA** package.
DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of the **die**-up flex **BGA** package.
IC die (102)
substrate (104)
wire bond (108)
stiffener (112)
opening (114)
bond pad (118)
contact pad (120)
pp; 79 DwgNo 4/51

53/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015041624
WPI Acc No: 2003-102140/200309
XRAM Acc No: C03-025610
XRPX Acc No: N03-081560

Ball grid array package to package and interface **integrated circuit die** with printed circuit board, has stiffener/**heat spreader**, substrate with window-shaped aperture, **integrated circuit die**, and drop-in **heat spreader**

Patent Assignee: BROADCOM CORP (BROA-N)
Inventor: KHAN R R; ZHAO S Z

Number of Countries: 102 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020109226	A1	20020815	US 2001783034	A	20010215	200309	B
WO 200267321	A2	20020829	WO 2002US2207	A	20020125	200309	
EP 1374305	A2	20040102	EP 2002702083	A	20020125	200409	
			WO 2002US2207	A	20020125		
TW 560019	A	20031101	TW 2002101690	A	20020131	200425	
AU 2002235468	A1	20020904	AU 2002235468	A	20020125	200427	

Priority Applications (No Type Date): US 2001783034 A 20010215
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020109226	A1		16	H01L-021/44	
WO 200267321	A2	E		H01L-023/00	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VN YU ZA ZM ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZM ZW

EP 1374305	A2	E		H01L-023/498	Based on patent WO 200267321

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR

TW 560019	A			H01L-023/28	
AU 2002235468	A1			H01L-023/00	Based on patent WO 200267321

Abstract (Basic): US 20020109226 A1
Abstract (Basic):

NOVELTY - A **ball grid array** package comprises a stiffener/**heat spreader**, a substrate with a central window-shaped aperture extending through the substrate, an **integrated circuit die** mounted to accessible portion of the stiffener/**heat spreader**, and a drop-in **heat spreader** having a surface mounted to the second **IC die** surface.

DETAILED DESCRIPTION - A **ball grid array** package comprises a stiffener/**heat spreader**, a substrate (104) having a central window-shaped aperture (112) extending through the substrate from its first surface to second surface, an **integrated circuit** (**IC**) **die** (102) mounted to an accessible portion of the stiffener/**heat spreader**, and a drop-in **heat spreader** having a surface mounted to the second **IC die** surface. The first substrate surface is **attached** to a surface of the stiffener (110)/**heat spreader**. A portion of the stiffener/**heat spreader** is accessible through the central window-shaped aperture.

INDEPENDENT CLAIMS are included for the following:
(a) a method of assembling a **ball grid array** package;and
(b) a system for assembling a **ball grid array** package.
USE - To package and interface an **integrated circuit die** (preferably high speed ICs) with a printed circuit board.
ADVANTAGE - The invention has improved **heat spreading** capabilities and reduces thermal stress during the assembly processes, thus improving packaging yields. It also has an improved mechanical, thermal, and electrical performance.
DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of a **ball grid array** package.
Die (102)
Substrate (104)
Window-shaped aperture (112)
Epoxy (134, 204)
pp; 16 DwgNo 2A/6

53/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015028509
WPI Acc No: 2003-089026/200308
XRAM Acc No: C03-022553
XRPX Acc No: N03-070089
Semiconductor device production comprises filling recess with conductive material to form plug, forming active device, applying insulator layer on active device and plug, and forming conductive path
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: TONTI W R; VOLDMAN S H
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6432809	B1	20020813	US 2000514396	A	20000228	200308	B

Priority Applications (No Type Date): US 2000514396 A 20000228
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6432809	B1		8	H01L-021/44	

Abstract (Basic): US 6432809 B1
Abstract (Basic):
NOVELTY - A semiconductor device is formed by forming a recess in a substrate having a thermal barrier. The recess is filled with a **thermally conductive** material to form a plug. An active device is formed at the substrate surface adjacent to the plug. An insulator layer is applied on the active device and plug. A conductive path is formed from the plug to the insulator layer.
DETAILED DESCRIPTION - The production of a semiconductor device involves forming a recess in a substrate having a thermal barrier. The recess extends through the **thermal** barrier and into **conductive** material of the substrate underlying the thermal barrier. An electrical insulator is formed in the recess. It has less thermal resistance than the thermal barrier. The recess is filled with a **thermally conductive** material to form a plug. An insulator layer is applied on the active device and the plug. A **thermally conductive** path is formed from the plug through

the insulator layer to a surface of the insulator layer.

USE - For the production of a semiconductor device, e.g. a silicon-on-insulator **integrated circuit**.

ADVANTAGE - The semiconductor device has increased heat dissipation properties. The thermal poly plug structure of the device provides power dissipation needed by highest levels of performance and greatest density of integration, and avoids trade-offs between power dissipation requirements and **chip** functionality and performance. The conducting paths increase the **conduction** of **heat** through the **chip** to allow greater control of heat distribution and temperature regulation across the **chip** to limit local temperature excursions in the **chip**.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of the semiconductor device with a passive heat sink or active cooling device.

Pad (38)

Heat sink (46)

pp; 8 DwgNo 3/4

53/3,AB/6 (Item 6 from file: 350)

DIALOG(R)File 350:Derwent WPIX

014814659

WPI Acc No: 2002-635365/200268

Related WPI Acc No: 2002-635363; 2003-420004; 2003-620193; 2003-678809; 2003-678811; 2003-678812; 2003-720751; 2004-080035; 2004-080038; 2004-080065; 2004-080066; 2004-256081; 2004-256082

XRAM Acc No: C02-179222

XRPX Acc No: N02-501902

Ball grid array package for **integrated circuit** devices, has substrate, stiffener, **integrated circuit die**, **heat spreader**, and **solder balls**

Patent Assignee: BROADCOM CORP (BROA-N); BACHER B (BACH-I); KHAN R R (KHAN-I); ZHAO S Z (ZHAO-I)

Inventor: BACHER B; KHAN R R; ZHAO S Z

Number of Countries: 002 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020079572	A1	20020627	US 2000742366	A	20001222	200268	B
TW 517359	A	20030111	TW 2001129877	A	20011203	200356	

Priority Applications (No Type Date): US 2000742366 A 20001222; US 2001984259 A 20011029

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020079572	A1		36	H01L-023/10	
TW 517359	A			H01L-023/28	

Abstract (Basic): US 20020079572 A1

Abstract (Basic):

NOVELTY - A **ball grid array** package comprises a substrate with first and second surfaces; a stiffener having first and second surfaces; an **integrated circuit die** having first and second surfaces; a **heat spreader** having a first surface mounted to the second **die** surface; and **solder balls attached** to the second substrate surface.

DETAILED DESCRIPTION - A **ball grid array** (

BGA) package comprises a substrate (104) having first and second surfaces; a stiffener (112) having a first surface and a second surface **attached** to the first substrate surface; an **integrated circuit** (**IC**) **die** (102) having a first surface mounted to the first stiffener surface and a second surface; a **heat spreader** (402) having a first surface mounted to the second **IC die** surface; and **solder balls** (106) **attached** to the second substrate surface. An INDEPENDENT CLAIM is included for a method of assembling the **BGA** package, comprising providing a tape substrate; **attaching** the first stiffener surface to the first substrate surface; mounting the **IC die** to the second stiffener surface; mounting the **heat spreader** to the **IC die**; and **attaching** the **solder balls** to the second substrate surface.

USE - For packaging **integrated circuit** devices.

ADVANTAGE - The inventive package has **enhanced electrical** and **thermal** characteristics, preferably improved **heat spreading** capabilities while also providing for high levels of **IC** electrical performance.

DESCRIPTION OF DRAWING(S) - The figure illustrates a cross-sectional view of a **die**-up flex **BGA** package.

Integrated circuit die (102)
Substrate (104)
Solder balls (106)
Wire bond (108)
Stiffener (112)
Contact pad (118)
Heat spreader (402)
pp; 36 DwgNo 4/21

53/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014446234
WPI Acc No: 2002-266937/200231
Related WPI Acc No: 2002-224460; 2004-478137
XRPX Acc No: N02-207472

Ceramic **IC** package for **ball grid** arrays has stackable structure with cavity holding semiconductor **die**

Patent Assignee: CORISIS D J (CORI-I); KINSMAN L D (KINS-I); MESS L E (MESS-I); MODEN W L (MODE-I); MICRON TECHNOLOGY INC (MICR-N)
Inventor: CORISIS D J; KINSMAN L D; MESS L E; MODEN W L
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20010048152	A1	20011206	US 9891205	P	19980630	200231	B
			US 99344279	A	19990630		
			US 2001924635	A	20010808		
US 6650007	B2	20031118	US 9891205	P	19980630	200376	
			US 99344279	A	19990630		
			US 2001924635	A	20010808		

Priority Applications (No Type Date): US 9891205 P 19980630; US 99344279 A 19990630; US 2001924635 A 20010808
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010048152	A1		14	H01L-023/02	Provisional application US 9891205

			Cont of application US 99344279
			Cont of patent US 6297548
US 6650007	B2	H01L-023/02	Provisional application US 9891205
			Cont of application US 99344279
			Cont of patent US 6297548

Abstract (Basic): US 20010048152 A1

Abstract (Basic):

NOVELTY - **BGA** package holds semiconductor **die** (14) in recess with **wire bonds** (26) linked to tracks on upper surface (20). **Die** is encapsulated in cavity after bonding to package which includes frustoconical lip (38) allowing packages to stack easily. Base contact bumps are formed as reflowed **solder balls** (50).

DETAILED DESCRIPTION - Top and bottom carrier surfaces are **connected** by an internal circuit (34). Heat sink fins (42) may protrude from the edge of the package.

USE - Used for packaging BGAs in a stacked arrangement for **IC** manufacture.

ADVANTAGE - Allows **high temperature** operation of BGAs while minimizing lead length from **die** to PCB.

DESCRIPTION OF DRAWING(S) - The drawing shows a stackable **BGA** package.

Substrate (2)
Assembly of packages (10)
Individual stackable **BGA** package (12)
Semiconductor **die** (14)
Contact pads (18)
Upper surface of carrier (20)
Lower surface of carrier (22)
Wire bonds (26)
Bond pads (28)
Internal circuit (34)
Frustoconical recess surface (36)
Frustoconical lip (38)
Heat transfer fins (42)
Solder balls (50)
pp; 14 DwgNo 1/6

53/3,AB/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014300230
WPI Acc No: 2002-120934/200216
Related WPI Acc No: 2001-464313; 2001-520884; 2001-548933; 2002-065861; 2002-120893; 2002-518300; 2003-310571; 2003-720224; 2004-040387
XRAM Acc No: C02-036888
XRPX Acc No: N02-090687

Fabrication of leadless **integrated circuit** package by etching leadframe strip to define **contact pads, wire bonding** semiconductor **die** to pads, and singulating leadless **integrated circuit** package from strip

Patent Assignee: ASAT LTD (ASAT-N)
Inventor: FAN N; MCLELLAN N
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6294100	B1	20010925	US 9895803	A	19980610	200216	B

US 99288352 A 19990408
US 99454794 A 19991203

Priority Applications (No Type Date): US 99454794 A 19991203; US 9895803 A 19980610; US 99288352 A 19990408
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6294100	B1		7	C23F-001/00	CIP of application US 9895803 CIP of application US 99288352

Abstract (Basic): US 6294100 B1
Abstract (Basic):

NOVELTY - A leadless **integrated circuit** package is fabricated by etching a leadframe strip to define **contact pads**; **attaching** an **adhesive film** to a bottom surface of the strip; **wire bonding** a mounted semiconductor **die** to the pads; **solder** plating the exposed bottom surface; and singulating the leadless **integrated circuit** package from the strip.

DETAILED DESCRIPTION - Fabrication of a leadless **integrated circuit** package includes;

(a) etching a leadframe strip to define **contact pads** (203);

(b) **attaching** an **adhesive film** to a bottom surface of the strip;

(c) mounting a semiconductor **die** (206) to the film intermediate respective pairs of the pads;

(d) **wire bonding** the **die** to the respective pairs of the pads;

(e) encapsulating a top surface of the strip in a molding material;

(f) removing the film from the bottom surface of the strip for exposing the pads and the **die**;

(g) **solder** plating the exposed bottom surface of the strip; and

(h) singulating the leadless **integrated circuit** package from the strip, where the film holds the **die** in place before the encapsulating step, and prevents the molding material from **contacting** the exposed **contact pads**.

USE - For fabricating leadless **integrated circuit** package (claimed).

ADVANTAGE - The invention does not require a **die attach** pad. It has a low package profile, extremely small **integrated circuit** package assembly, availability of corner areas of the package for additional input/output, and optional **soldering** of the exposed **die** to a circuit mother board for **enhanced thermal** performance.

DESCRIPTION OF DRAWING(S) - The figure shows a processing step of manufacturing an exposed **die** leadless plastic **chip** carrier (EDLPCC).

Contact pads (203)
Wires (205)
Semiconductor **die** (206)
Over mold (401)
pp; 7 DwgNo 1E/2

53/3,AB/9 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012774651
WPI Acc No: 1999-580878/199949
XRPX Acc No: N99-428855
Cooling system for an **integrated circuit** (**IC**) package such as an infrared radiation detector
Patent Assignee: RAYTHEON CO (RAYT)
Inventor: MEISSNER E G
Number of Countries: 086 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9950910	A1	19991007	WO 99US7165	A	19990331	199949	B
AU 9932196	A	19991018	AU 9932196	A	19990331	200010	
US 6043982	A	20000328	US 9853573	A	19980401	200023	
EP 1070350	A1	20010124	EP 99914320	A	19990331	200107	
			WO 99US7165	A	19990331		
JP 2002510864	W	20020409	WO 99US7165	A	19990331	200227	
			JP 2000541736	A	19990331		
EP 1070350	B1	20030917	EP 99914320	A	19990331	200369	
			WO 99US7165	A	19990331		
DE 69911390	E	20031023	DE 611390	A	19990331	200377	
			EP 99914320	A	19990331		
			WO 99US7165	A	19990331		

Priority Applications (No Type Date): US 9853573 A 19980401
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9950910	A1	E	27	H01L-023/38	

Designated States (National): AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SL SZ UG ZW

AU 9932196	A				Based on patent WO 9950910
US 6043982	A			H05K-007/20	
EP 1070350	A1	E		H01L-023/38	Based on patent WO 9950910

Designated States (Regional): DE FR GB IT NL SE

JP 2002510864	W		26	H01L-023/38	Based on patent WO 9950910
EP 1070350	B1	E		H01L-023/38	Based on patent WO 9950910

Designated States (Regional): DE FR GB IT NL SE

DE 69911390	E			H01L-023/38	Based on patent EP 1070350
					Based on patent WO 9950910

Abstract (Basic): WO 9950910 A1
Abstract (Basic):

NOVELTY - Thermoelectric cooling (TEC) elements (51) are disposed between an **IC** support (12) and a base (36). The TEC elements are electrically **connected** in series by metal leads (47,48) provided on opposing surfaces of the support and the base. Electrically conductive elements (44) are between the support and the base and bonded to metal **pads** (32,42) to **contact** conductive layers (29,38).

DETAILED DESCRIPTION - An **IC** (13) is fixed on the support by a thin **thermally conductive solder** film (14) and is electrically **connected** to **leads** (17) by **wire bonds** (18). A **frame** (22) extends around the circuit and a plate-like window (23) is **sealed** to the frame to form a chamber which is maintained in a vacuum state.

USE - For **IC** packages such as an infrared radiation detector.

ADVANTAGE - Avoids the need for relatively long **wire**

bonds, while mechanically strengthening the interconnection between the **IC** support and the base. Avoids outgassing of the TEC elements since they are not contained within the **IC** chamber. Facilitates rapid and accurate assembly of a package since n-type TEC elements of different C/D shapes are used.

DESCRIPTION OF DRAWING(S) - The figure shows a sectional side view of an **IC** package with the cooling system.

IC support (12)
IC (13)
Solder film (14)
Leads (17)
Wire bonds (18)
Frame (22)
Plate-like window (23)
Chamber (25)
Conductive layers (29,38)
Metal pads (32,42)
Base (36)
Electrically conductive elements (44)
Metal leads (47,48)
Elements (51)
pp; 27 DwgNo 1/5

53/3,AB/10 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012029359
WPI Acc No: 1998-446269/199838
XRAM Acc No: C98-135390
XRPX Acc No: N98-347832

Thermally enhanced micro-**ball grid array** package - has an electrically conductive cap which provides means for **connecting** the **die** to other electrical elements and dissipates heat

Patent Assignee: NAT SEMICONDUCTOR CORP (NASC)
Inventor: JOSHI R
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5789809	A	19980804	US 95517603	A	19950822	199838	B

Priority Applications (No Type Date): US 95517603 A 19950822
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5789809	A		7	H01L-023/12	

Abstract (Basic): US 5789809 A

A **thermally enhanced** micro-**ball grid array** package (102) includes an electrically conductive cap (80), and a **die** (104) **attached** by an electrically conductive epoxy, and has an output terminal (110) **connected** to the cap. The bottom surface (108) of the **die** includes a central portion (112) and a peripheral portion (114) with input/output terminals (116). A shock-absorbing **elastomer layer** (12) centrally **attached** to the bottom surface of the **die** includes a polyimide film (122) with **contact pads** (130) on its top surface (124). They are **connected** to terminals (116) by **bonding wires** (134) surrounded by an encapsulating material

(136), and **connected** to bumps (128) formed from an alloy including nickel and gold on its bottom surface (126) by traces (132).

ADVANTAGE - Eliminates the need for a lead-frame, and provides enhanced heat dissipation characteristics.

Dwg.4/4

53/3,AB/11 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010262509
WPI Acc No: 1995-163764/199522
XRAM Acc No: C95-075746
XRPX Acc No: N95-128455

Soldering conductor cable to circuit board - by applying heated tip to **solder** through covering heat resistant **adhesive** tape to prevent contamination

Patent Assignee: NEC CORP (NIDE)
Inventor: TAKAHASHI H; TAKASHI H
Number of Countries: 006 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 651463	A2	19950503	EP 94116730	A	19941024	199522	B
AU 9477472	A	19950518	AU 9477472	A	19941025	199528	
JP 7130225	A	19950519	JP 93270831	A	19931028	199529	
US 5478008	A	19951226	US 94324613	A	19941018	199606	
EP 651463	A3	19961016	EP 94116730	A	19941024	199648	
AU 673626	B	19961114	AU 9477472	A	19941025	199702	
EP 651463	B1	19990512	EP 94116730	A	19941024	199923	
DE 69418420	E	19990617	DE 618420	A	19941024	199930	
			EP 94116730	A	19941024		

Priority Applications (No Type Date): JP 93270831 A 19931028
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 651463	A2	E	6	H01R-004/02	
Designated States (Regional): DE FR GB					
JP 7130225	A		3	H01B-007/08	
US 5478008	A		5	H01L-021/603	
AU 673626	B			H05K-003/34	Previous Publ. patent AU 9477472
EP 651463	B1	E		H01R-004/02	
Designated States (Regional): DE FR GB					
DE 69418420	E			H01R-004/02	Based on patent EP 651463
AU 9477472	A			H05K-003/34	
EP 651463	A3			H01R-004/02	

Abstract (Basic): EP 651463 A

Electric conductor wire is **soldered** to an electronic circuit board by: (a) contacting the exposed conductor core tip with the **contact pad** of the circuit board, and covering both the exposed core tip, and the end of the insulation coating with a heat resistive **adhesive** tape; and (b) applying the heater tip to the tape at the point covering the **conductor** core end to **melt** the **solder** on the circuit board by heating through the tape and thus form a **soldered** joint with the conduction core.

USE - In forming a **soldered joint** between a conductor **wire** and an electronic circuit board, particularly when using a heater **chip** of a heated **soldering** unit.

ADVANTAGE - The covering tape prevents melting of wire insulation

and also prevents **solder** dregs adhering to the **solder** tip, causing contamination of the surface of the circuit boards.
Dwg.2/4

Abstract (Equivalent): US 5478008 A
A **soldering** method for **soldering** an electric cable to a wiring pattern of a circuit board, comprising:
contacting an exposed top portion of a core conductor of the electric cable, having a heat-resistive **adhesive** tape stuck on the exposed top portion of the core conductor and an edge of an insulating coating of the electric cable, with a **solder connecting** point of a wiring pattern; and
soldering the core conductor to the **solder connecting** point by heating it while contacting a heater tip with the heat-resistive **adhesive** tape on the core conductor.
Dwg.0/4

53/3,AB/12 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

03831474
LEAD FRAME

PUB. NO.: 04-196574 [JP 4196574 A]
PUBLISHED: July 16, 1992 (19920716)
INVENTOR(s): SAKANO RYUICHI
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-331348 [JP 90331348]
FILED: November 28, 1990 (19901128)
JOURNAL: Section: E, Section No. 1286, Vol. 16, No. 526, Pg. 39, October 28, 1992 (19921028)

ABSTRACT

PURPOSE: To prevent creeping-up of a **brazing** material onto a hanging lead and to enhance reliability by providing a **brazing** material reservoir for reserving flowing **brazing** material when the material overflows on the lead so as to bring a **chip** into close **contact** with a **die pad**.

CONSTITUTION: A **brazing** material 8 is placed on a **die** pad 3 to heat the pad 3 to a **high temperature** thereby to melt the material 8. A **chip** 5 is placed on the material 8 in this state, and brought into close **contact** with the **pad** 3. In this case, since the **chip** 5 is formed in a shape for pressing the material 8 from above, the material 8 is extended from the **chip** 5 to flow on the pad 3, the material 8 flows to a **brazing** material reservoir 9 becoming a further **higher temperature** on a hanging lead 4, and the material 8 reserved in the reservoir 9 is stopped thereby. Then, bonding pads 6, inner leads 2 or the leads 4 on the **chip** 5 are **wire bonded** by wiring 7.

```
SYSTEM:OS  - DIALOG OneSearch
  File   2:INSPEC 1969-2004/Jul W3
         (c) 2004 Institution of Electrical Engineers
*File   2: Alert feature enhanced for multiple files, duplicates
removal, customized scheduling. See HELP ALERT.
  File   6:NTIS 1964-2004/Jul W4
         (c) 2004 NTIS, Intl Cpyrght All Rights Res
  File   8:Ei Compendex(R) 1970-2004/Jul W3
         (c) 2004 Elsevier Eng.  Info. Inc.
  File  34:SciSearch(R) Cited Ref Sci 1990-2004/Jul W3
         (c) 2004 Inst for Sci Info
  File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
  File  35:Dissertation Abs Online 1861-2004/May
         (c) 2004 ProQuest Info&Learning
  File  65:Inside Conferences 1993-2004/Jul W4
         (c) 2004 BLDSC all rts. reserv.
  File  94:JICST-EPlus 1985-2004/Jul W1
         (c)2004 Japan Science and Tech Corp(JST)
  File  99:Wilson Appl. Sci & Tech Abs 1983-2004/Jun
         (c) 2004 The HW Wilson Co.
  File 144:Pascal 1973-2004/Jul W3
         (c) 2004 INIST/CNRS
  File 305:Analytical Abstracts 1980-2004/Jul W3
         (c) 2004 Royal Soc Chemistry
*File 305: Alert feature enhanced for multiple files, duplicate
removal, customized scheduling.  See HELP ALERT.
  File 315:ChemEng & Biotec Abs 1970-2004/Jun
         (c) 2004 DECHEMA
  File 350:Derwent WPIX 1963-2004/UD,UM &UP=200447
         (c) 2004  Thomson Derwent
*File 350: For more current information, include File 331 in your search.
Enter HELP NEWS 331 for details.
  File 347:JAPIO Nov 1976-2004/Mar(Updated 040708)
         (c) 2004 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed.
Alerts have been run.  See HELP NEWS 347 for details.
  File 344:Chinese Patents Abs Aug 1985-2004/May
         (c) 2004 European Patent Office
  File 371:French Patents 1961-2002/BOPI 200209
         (c) 2002 INPI.  All rts. reserv.
*File 371: This file is not currently updating. The last update is 200209.
```

Set	Items	Description
S1	10035	AU=(ZHANG, T? OR ZHANG T?)
S2	2241	AU=(KHAN, R? OR KHAN R?)
S3	12275	S1:S2
S4	23	S3 AND (SOLDER(W)BOND? OR SOLDER OR SOLDERING OR SOLDERED - OR BRAZ?)
S5	13	S4 AND ((SOLDER?)(W)(BALL? ? OR BUMP? ? OR POST? ? OR SPHERE? OR PAD OR PADS OR PLATE?) OR BGA OR BALLGRID? ? OR BALL(W)GRID? ? OR POLYMER(W)BALL? ?)
S6	13	RD (unique items)
S7	10	S4 NOT S5
S8	10	RD (unique items)
S9	0	S8 AND ((HEAT? OR WARM? OR HOT? OR CALEFACT? OR TORREFACT? OR PYROL? OR SINTER? OR CALCIN? OR AUTOCLAV?)(3N)(CONDUCT? OR SPREAD?))
S10	10	S8

6/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

016340107
WPI Acc No: 2004-498004/200447
Related WPI Acc No: 2004-009777
XRAM Acc No: C04-184418
XRPX Acc No: N04-393271
Integrated circuit package, e.g. **ball grid** array package for die-up and die-down orientations, comprises first substrate surface attached to first surface of stiffener, and second substrate surface attached to second surface of stiffener
Patent Assignee: BROADCOM CORP (BROA-N)
Inventor: CHAUDHRY I; **KHAN R R**; ZHAO S Z
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20040113284	A1	20040617	US 2002101751	A	20020321	200447 B
			US 2003730093	A	20031209	

Priority Applications (No Type Date): US 2002101751 A 20020321; US 2003730093 A 20031209
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20040113284	A1		52	H01L-023/48	Div ex application US 2002101751

Abstract (Basic): US 20040113284 A1
Abstract (Basic):
NOVELTY - An integrated circuit (IC) package comprises first substrate (104); second substrate (502); and stiffener (112).
A surface of the first substrate is attached to a first surface of the stiffener, and a surface of the second substrate is attached to a second surface of the stiffener.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for:
(a) a method of assembling a **ball grid** array (**BGA**) package (402, 500) comprising attaching a surface of a first substrate to a first surface of a stiffener; and attaching a surface of a second substrate to a second surface of the stiffener; and
(b) a method of making IC packages comprising forming a stiffener strip that includes stiffeners; forming a first substrate strip that includes first substrates; forming a second substrate strip that includes second substrates; laminating the first substrate strip to a first surface of the stiffener strip; and laminating the second substrate strip to a second surface of the stiffener strip, where a substrate/stiffener/substrate strip combination is created.
USE - The IC package, e.g. **BGA** package is used for die-up and die-down orientations.
ADVANTAGE - The IC package has improved heat-spreading capabilities while providing greater routing capacity and higher levels of IC electrical performance.
DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of a **BGA** package.
Package (100)
Die (102)
Substrate (104, 502)
Stiffener (112)
Thermal connector (404)
BGA package (500)
pp; 52 DwgNo 5/21

6/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

016098206
WPI Acc No: 2004-256082/200424
Related WPI Acc No: 2002-635363; 2002-635365; 2003-420004; 2003-620193; 2003-678809; 2003-678811; 2003-678812; 2003-720751; 2004-080035; 2004-080038; 2004-080065; 2004-080066; 2004-256081
XRAM Acc No: C04-099952
XRPX Acc No: N04-203516
Ball grid array package for printed circuit board, has **solder balls** attached to bottom of tape substrate mounted with stiffener, integrated circuit die and heat spreader, sequentially
Patent Assignee: KHAN R R (KHAN-I); ZHAO S Z (ZHAO-I)
Inventor: **KHAN R R**; ZHAO S Z
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020185722	A1	20021212	US 2000742366	A	20001222	200424 B
			US 2002201891	A	20020725	

Priority Applications (No Type Date): US 2000742366 A 20001222; US 2002201891 A 20020725
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020185722	A1		37	H01L-023/02	Div ex application US 2000742366

Abstract (Basic): US 20020185722 A1
Abstract (Basic):
NOVELTY - A tape substrate (104) is mounted with the stiffener, integrated circuit (IC) die (102) and heat spreader, sequentially. Several **solder balls** (106) are attached to the bottom of the substrate.
DETAILED DESCRIPTION - The heat spreader dissipates heat generated by IC die attached through silver filled epoxy (116). The heat spreader contact area of die, is greater than that of heat spreader. The heat spreader has a surface which forms specific exposed surface of the package. An INDEPENDENT CLAIM is also included for assembling method of **ball grid** array (**BGA**) package which involves reducing thermal stress at interface of IC die and stiffener surface, during operation of die.
USE - For printer circuit board.
ADVANTAGE - Improves IC electrical performance and heat spreading capabilities of the package.
DESCRIPTION OF DRAWING(S) - The figure shows a sectional view of the **BGA** package.
IC die (102)
substrate (104)
solder balls (106)
BGA package (110)
stiffener (112)
openings (114)
silver filled epoxy (116)
pp; 37 DwgNo 1B/21

6/3,AB/3 (Item 3 from file: 350)

DIALOG(R)File 350:Derwent WPIX

016098205
WPI Acc No: 2004-256081/200424
Related WPI Acc No: 2002-635363; 2002-635365; 2003-420004; 2003-620193; 2003-678809; 2003-678811; 2003-678812; 2003-720751; 2004-080035; 2004-080038; 2004-080065; 2004-080066; 2004-256082
XRAM Acc No: C04-099951
XRPX Acc No: N04-203515

Ball-grid array package for high-speed application specific integrated circuit, has heat spreader mounted on integrated circuit die, dissipates heat generated by die

Patent Assignee: BACHER B (BACH-I); KHAN R R (KHAN-I); ZHAO S Z (ZHAO-I)
Inventor: BACHER B; **KHAN R R**; ZHAO S Z

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020185720	A1	20021212	US 2000742366	A	20001222	200424 B
			US 2002197438	A	20020718	

Priority Applications (No Type Date): US 2000742366 A 20001222; US 2002197438 A 20020718
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020185720	A1		36	H01L-023/02	Div ex application US 2000742366

Abstract (Basic): US 20020185720 A1
Abstract (Basic):

NOVELTY - A tape/organic substrate (104) has stiffener (112) on which an integrated circuit (IC) die (102) is mounted by silver filled epoxy (116). A heat spreader (402) mounted on die center dissipates heat generated by die. Several **solder balls** (106) connected to ground potential, are attached to substrate lower surface and to stiffener through a conductive material filled via extending through substrate.

DETAILED DESCRIPTION - The wire bonds (108) provided corresponding to bond pads (118) formed on IC die, couples bond pad to stiffener lower surface into which an opening (114) is extending from upper surface. Another wire bond couples another bond pad to metal layer by extending through the stiffener openings so as to connect to substrate via. The substrate has window opening which exposes portion of stiffener lower surface which is configured to be coupled with printed circuit board (PCB) such that the PCB is coupled to heat spreader whose upper surface is plated with **solder**. The stiffener has a centrally-located cavity which protrudes through window opening and which is plated with **solder** such that the stiffener is surface mounted to **soldering pad** of PCB. A metal ring is attached to stiffener upper surface to which ground pad of IC die is coupled by ground wire bond, so as to dissipate heat from stiffener. A stud bridges stiffener across wire bond opening extending through stiffener. A plated die-attach pad centered on the substrate, is configured to mount the IC die. An INDEPENDENT CLAIM is also included for **ball grid** array package assembling method.

USE - **Ball grid** array (**BGA**) package e.g. ceramic **BGA** package, plastic **BGA** (PBGA) package, flex **BGA** package, die-up and die-down **BGA** packages, for high speed application specific integrated circuits (ASIC).

ADVANTAGE - By providing the heat spreader, the heat spreading and dissipating capabilities are improved.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of die-up flex **BGA** package.
IC die (102)
tape/organic substrate (104)
solder balls (106)
wire bonds (108)
stiffener (112)
epoxy (116,404)
stiffener openings (114)
bond pads (118)
contact points (120)
heat spreader (402)
pp; 36 DwgNo 4/21

6/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015922225
WPI Acc No: 2004-080065/200408
Related WPI Acc No: 2002-635363; 2002-635365; 2003-420004; 2003-620193; 2003-678809; 2003-678811; 2003-678812; 2003-720751; 2004-080035; 2004-080038; 2004-080066; 2004-256081; 2004-256082
XRAM Acc No: C04-032727
XRPX Acc No: N04-063958
Die-up **ball grid** array package for integrated circuit includes heat spreader and **solder balls** mounted and attached on upper and lower surfaces of integrated circuit die and tape substrate
Patent Assignee: KHAN R R (KHAN-I); ZHAO S Z (ZHAO-I)
Inventor: **KHAN R R**; ZHAO S Z
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020190361	A1	20021219	US 2000742366	A	20001222	200408 B
			US 2002200255	A	20020723	

Priority Applications (No Type Date): US 2000742366 A 20001222; US 2002200255 A 20020723
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020190361	A1		37	H01L-023/02	Div ex application US 2000742366

Abstract (Basic): US 20020190361 A1
Abstract (Basic):
NOVELTY - An integrated circuit die (102) is arranged on an upper surface of a stiffener (112) which is mounted on the upper surface of a tape substrate (104). A heat spreader (402) is mounted on the surface of the integrated circuit (IC) die. The **solder balls** (106) are attached to the lower surface of the substrate
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for **ball grid** array package assembly.
USE - Used in field of integrated circuit (IC) device packaging technology e.g. for IC dies using printed circuit board.
ADVANTAGE - Thermal stress at the interface of the IC die and stiffener can be substantially released or altered by heat spreader and the deformation caused by thermal stress in the stiffener and substrate can also be reduced.
DESCRIPTION OF DRAWING(S) - The figure shows a cross-section of the die up flexible **ball grid** array package.

Integrated circuit die (102)
Tape substrate (104)
Solder ball (106)
Stiffener (112)
Heat spreader (402)
pp; 37 DwgNo 4/21

6/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015922198
WPI Acc No: 2004-080038/200408
Related WPI Acc No: 2002-635363; 2002-635365; 2003-420004; 2003-620193; 2003-678809; 2003-678811; 2003-678812; 2003-720751; 2004-080035; 2004-080065; 2004-080066; 2004-256081; 2004-256082
XRAM Acc No: C04-032700
XRPX Acc No: N04-063940
Ball grid array package for integrated circuit devices, has substrate, stiffener, integrated circuit die, heat spreader, and **solder balls**
Patent Assignee: BACHER B (BACH-I); KHAN R R (KHAN-I); ZHAO S Z (ZHAO-I)
Inventor: BACHER B; **KHAN R R**; ZHAO S Z
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020185750	A1	20021212	US 2000742366	A	20001222	200408 B
			US 2002200336	A	20020723	

Priority Applications (No Type Date): US 2000742366 A 20001222; US 2002200336 A 20020723
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020185750	A1		37	H01L-023/48	Div ex application US 2000742366

Abstract (Basic): US 20020185750 A1
Abstract (Basic):
NOVELTY - An electrically and thermally enhanced die-up tape substrate **ball grid** array (**BGA**) package and die-up plastic substrate **BGA** package.
DETAILED DESCRIPTION - A **BGA** package comprises:
(i) a substrate that has a first and second surface;
(ii) a stiffener that has a first and second surface joined to substrate;
(iii) an IC die mounted on first stiffener surface;
(iv) a heat sink mounted on second IC surface;
(v) a number of **solder balls** joined to second substrate surface.
The package comprises silver-filled epoxy.
USE - An electrically and thermally enhanced die-up tape substrate **ball grid** array (**BGA**) package and die-up plastic substrate **BGA** package.
ADVANTAGE - Assembly has reduced thermal stress between components with different thermal co-efficients due to heat dissipation.
DESCRIPTION OF DRAWING(S) - Drawing shows conventional flex **BGA** package.
(100) Flex **BGA** package;
(102) IC die;
(104) tape substrate;

(106) **solder balls**;
(108) wire bonds;
(116) epoxy;
(118) bond pads;
(120) contact points.
pp; 37 DwgNo 1/21

6/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015922195
WPI Acc No: 2004-080035/200408
Related WPI Acc No: 2002-635363; 2002-635365; 2003-420004; 2003-620193; 2003-678809; 2003-678811; 2003-678812; 2003-720751; 2004-080038; 2004-080065; 2004-080066; 2004-256081; 2004-256082
XRAM Acc No: C04-032697
XRPX Acc No: N04-063937
Ball grid array package for integrated circuit devices, has substrate, stiffener, integrated circuit die, heat spreader, and **solder balls**
Patent Assignee: KHAN R R (KHAN-I); ZHAO S Z (ZHAO-I)
Inventor: **KHAN R R**; ZHAO S Z
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020185734	A1	20021212	US 2000742366	A	20001222	200408 B
			US 2002201893	A	20020725	

Priority Applications (No Type Date): US 2000742366 A 20001222; US 2002201893 A 20020725
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020185734	A1		37	H01L-021/48	Div ex application US 2000742366

Abstract (Basic): US 20020185734 A1
Abstract (Basic):
NOVELTY - **BGA** package comprises: a substrate (104) with first and second surfaces; a stiffener (112); an IC die (102) with a first surface mounted to the stiffener surface; a heat spreader mounted to the die; and **solder balls** (106) attached to the second substrate surface.
DETAILED DESCRIPTION - AN INDEPENDENT CLAIM is also included for: a method of assembling a **ball grid** array package, which comprises: providing a tape substrate (104) with the two surfaces; attaching the first surface of the stiffener (112) to the first substrate surface; mounting an IC die (102) to the second stiffener surface; mounting a heat spreader to the IC die; and attaching a number of **solder balls** to the second substrate surface.
USE - For substrate stiffening and heat spreading techniques in **BGA** packages.
ADVANTAGE - High levels of IC electrical performance are attained.
DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of a **BGA** package, with the heat spreader internal to the package.
IC die (102)
substrate (104)
solder balls (106)
stiffener (112)
bond pads on IC die (118)

contact points on substrate (120)
pp; 37 DwgNo 5/21

6/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015851950
WPI Acc No: 2004-009777/200401
Related WPI Acc No: 2004-498004
XRAM Acc No: C04-002632
XRPX Acc No: N04-007007
Ball grid array package for high-speed integrated circuits, has first substrate surface attached to first stiffener surface, and second substrate surface attached to second stiffener surface
Patent Assignee: BROADCOM CORP (BROA-N)
Inventor: CHAUDHRY I; **KHAN R R**; ZHAO S Z
Number of Countries: 032 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030179556	A1	20030925	US 2002101751	A	20020321	200401	B
EP 1351293	A2	20031008	EP 20036501	A	20030321	200401	

Priority Applications (No Type Date): US 2002101751 A 20020321
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030179556	A1		52	H05K-007/06	
EP 1351293	A2	E		H01L-023/31	

Designated States (Regional): AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LI LT LU LV MC MK NL PT RO SE SI SK TR

Abstract (Basic): US 20030179556 A1
Abstract (Basic):
NOVELTY - A **ball grid** array (**BGA**) package comprises two substrates (104, 502), and a stiffener (112). A surface of the first substrate is attached to a first surface of the stiffener, and a surface of the second substrate is attached to a second surface of the stiffener.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for assembling a **BGA** package.
USE - Used for high-speed ICs.
ADVANTAGE - The **BGA** packages have improved heat spreading capabilities, greater routing capacity and higher levels of IC electrical performance.
DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of a **BGA** package.
IC die (102)
Solder ball (106, 304)
Wire bond (108, 306, 806)
Via (302, 816)
pp; 52 DwgNo 8/21

6/3,AB/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015658566
WPI Acc No: 2003-720751/200368

Related WPI Acc No: 2002-635363; 2002-635365; 2003-420004; 2003-620193; 2003-678809; 2003-678811; 2003-678812; 2004-080035; 2004-080038; 2004-080065; 2004-080066; 2004-256081; 2004-256082
XRPX Acc No: N03-576219
Ball grid array package for integrated circuits, has stiffener attached to top surface of substrate having contact pads electrically connected to **solder ball** pads provided on substrate bottom surface
Patent Assignee: BROADCOM CORP (BROA-N)
Inventor: **KHAN R R**; ZHAO S Z
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030146511	A1	20030807	US 2002352877	P	20020201	200368 B
			US 2002284166	A	20021031	

Priority Applications (No Type Date): US 2002352877 P 20020201; US 2002284166 A 20021031
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030146511	A1		32	H01L-023/48	Provisional application US 2002352877

Abstract (Basic): US 20030146511 A1
Abstract (Basic):
NOVELTY - A stiffener (600) has an integrated circuit (IC) die (102) mounted on top surface (802). The bottom peripheral portion (804) of the stiffener covers an opening (702) provided on top surface (806) of another stiffener (700). The bottom surface (808) of the stiffener (700) is attached to top surface of a substrate (104) having contact pads which are electrically connected to **solder ball** pads (810) on substrate bottom surface.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for **ball grid** array assembling method.
USE - For packing high-speed integrated circuits.
ADVANTAGE - Improves thermal, electrical and mechanical characteristics of **ball grid** array package (**BGA**) package by providing more stiffeners. The **BGA** package having improved rigidity, greater heat transfer is realized by providing stiffeners.
DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of **ball grid** array package.
IC die (102)
substrate (104)
stiffeners (600,700)
opening (702)
top surfaces of stiffeners (802,806)
bottom surfaces of stiffeners (804,808)
solder ball pads (810)
pp; 32 DwgNo 9/18

6/3,AB/9 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015041624
WPI Acc No: 2003-102140/200309
XRAM Acc No: C03-025610
XRPX Acc No: N03-081560
Ball grid array package to package and interface integrated

circuit die with printed circuit board, has stiffener/heat spreader, substrate with window-shaped aperture, integrated circuit die, and drop-in heat spreader

Patent Assignee: BROADCOM CORP (BROA-N)
Inventor: **KHAN R R**; ZHAO S Z
Number of Countries: 102 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020109226	A1	20020815	US 2001783034	A	20010215	200309	B
WO 200267321	A2	20020829	WO 2002US2207	A	20020125	200309	
EP 1374305	A2	20040102	EP 2002702083	A	20020125	200409	
			WO 2002US2207	A	20020125		
TW 560019	A	20031101	TW 2002101690	A	20020131	200425	
AU 2002235468	A1	20020904	AU 2002235468	A	20020125	200427	

Priority Applications (No Type Date): US 2001783034 A 20010215
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020109226	A1		16	H01L-021/44	
WO 200267321	A2	E		H01L-023/00	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VN YU ZA ZM ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZM ZW

EP 1374305	A2	E		H01L-023/498	Based on patent WO 200267321

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR

TW 560019	A			H01L-023/28	
AU 2002235468	A1			H01L-023/00	Based on patent WO 200267321

Abstract (Basic): US 20020109226 A1
Abstract (Basic):

NOVELTY - A **ball grid** array package comprises a stiffener/heat spreader, a substrate with a central window-shaped aperture extending through the substrate, an integrated circuit die mounted to accessible portion of the stiffener/heat spreader, and a drop-in heat spreader having a surface mounted to the second IC die surface.

DETAILED DESCRIPTION - A **ball grid** array package comprises a stiffener/heat spreader, a substrate (104) having a central window-shaped aperture (112) extending through the substrate from its first surface to second surface, an integrated circuit (IC) die (102) mounted to an accessible portion of the stiffener/heat spreader, and a drop-in heat spreader having a surface mounted to the second IC die surface. The first substrate surface is attached to a surface of the stiffener (110)/heat spreader. A portion of the stiffener/heat spreader is accessible through the central window-shaped aperture.

INDEPENDENT CLAIMS are included for the following:

(a) a method of assembling a **ball grid** array package;and

(b) a system for assembling a **ball grid** array package.

USE - To package and interface an integrated circuit die (preferably high speed ICs) with a printed circuit board.

ADVANTAGE - The invention has improved heat spreading capabilities and reduces thermal stress during the assembly processes, thus improving packaging yields. It also has an improved mechanical, thermal, and electrical performance.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of a **ball grid** array package.
Die (102)
Substrate (104)
Window-shaped aperture (112)
Epoxy (134, 204)
pp; 16 DwgNo 2A/6

6/3,AB/10 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014922223
WPI Acc No: 2002-742930/200281
XRPX Acc No: N02-585290
Ball grid array package used for IC packaging, has heat spreader attached to substrate and several **solder balls** attached to the substrate outside the outer dimensional profile of the heat spreader
Patent Assignee: BROADCOM CORP (BROA-N)
Inventor: **KHAN R R; ZHANG T**
Number of Countries: 027 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1256980	A2	20021113	EP 2002252969	A	20020426	200281	B
US 20020171144	A1	20021121	US 2001849537	A	20010507	200301	

Priority Applications (No Type Date): US 2001849537 A 20010507
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1256980	A2	E	17	H01L-023/36	
	Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR				
US 20020171144	A1			H01L-023/52	

Abstract (Basic): EP 1256980 A2
Abstract (Basic):
NOVELTY - **Ball grid** array (**BGA**) package has a substrate (104) with a first and second surface, and a heat spreader (504) with first and second surface. The first surface of the heat spreader is attached to the second surface of the substrate. Several **solder balls** (106) are attached to the second substrate surface outside the outer dimensional profile of the heat spreader.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method of assembling a **ball grid** array package.
USE - Used for integrated circuit packaging.
ADVANTAGE - Provides a **BGA** package which has improved heat spreading capabilities and higher levels of IC electrical performance.
DESCRIPTION OF DRAWING(S) - The drawing illustrates a cross sectional view of a die up **BGA** package with heat spreader.
substrate (104)
heat spreader (504)
solder balls (106)
pp; 17 DwgNo 5/14

6/3,AB/11 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014814659
WPI Acc No: 2002-635365/200268
Related WPI Acc No: 2002-635363; 2003-420004; 2003-620193; 2003-678809; 2003-678811; 2003-678812; 2003-720751; 2004-080035; 2004-080038; 2004-080065; 2004-080066; 2004-256081; 2004-256082
XRAM Acc No: C02-179222
XRPX Acc No: N02-501902

Ball grid array package for integrated circuit devices, has substrate, stiffener, integrated circuit die, heat spreader, and **solder balls**

Patent Assignee: BROADCOM CORP (BROA-N); BACHER B (BACH-I); KHAN R R (KHAN-I); ZHAO S Z (ZHAO-I)
Inventor: BACHER B; **KHAN R R**; ZHAO S Z
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020079572	A1	20020627	US 2000742366	A	20001222	200268	B
TW 517359	A	20030111	TW 2001129877	A	20011203	200356	

Priority Applications (No Type Date): US 2000742366 A 20001222; US 2001984259 A 20011029
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020079572	A1		36	H01L-023/10	
TW 517359	A			H01L-023/28	

Abstract (Basic): US 20020079572 A1

Abstract (Basic):

NOVELTY - A **ball grid** array package comprises a substrate with first and second surfaces; a stiffener having first and second surfaces; an integrated circuit die having first and second surfaces; a heat spreader having a first surface mounted to the second die surface; and **solder balls** attached to the second substrate surface.

DETAILED DESCRIPTION - A **ball grid** array (**BGA**) package comprises a substrate (104) having first and second surfaces; a stiffener (112) having a first surface and a second surface attached to the first substrate surface; an integrated circuit (IC) die (102) having a first surface mounted to the first stiffener surface and a second surface; a heat spreader (402) having a first surface mounted to the second IC die surface; and **solder balls** (106) attached to the second substrate surface. An INDEPENDENT CLAIM is included for a method of assembling the **BGA** package, comprising providing a tape substrate; attaching the first stiffener surface to the first substrate surface; mounting the IC die to the second stiffener surface; mounting the heat spreader to the IC die; and attaching the **solder balls** to the second substrate surface.

USE - For packaging integrated circuit devices.

ADVANTAGE - The inventive package has enhanced electrical and thermal characteristics, preferably improved heat spreading capabilities while also providing for high levels of IC electrical performance.

DESCRIPTION OF DRAWING(S) - The figure illustrates a cross-sectional view of a die-up flex **BGA** package.

Integrated circuit die (102)
Substrate (104)
Solder balls (106)
Wire bond (108)
Stiffener (112)

Contact pad (118)
Heat spreader (402)
pp; 36 DwgNo 4/21

6/3,AB/12 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014814657
WPI Acc No: 2002-635363/200268
Related WPI Acc No: 2002-635365; 2003-420004; 2003-620193; 2003-678809; 2003-678811; 2003-678812; 2003-720751; 2004-080035; 2004-080038; 2004-080065; 2004-080066; 2004-256081; 2004-256082
XRPX Acc No: N02-501900
Enhanced die-up **BGA** package has thermal connector with first surface coupled to metal plane of substrate and second surface coupled to printed circuit board
Patent Assignee: BROADCOM CORP (BROA-N)
Inventor: BACHER B; **KHAN R R**; ZHAO S Z
Number of Countries: 101 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020079562	A1	20020627	US 2000742366	A	20001222	200268	B
			US 2001984259	A	20011029		
WO 200252645	A2	20020704	WO 2001US44952	A	20011130	200268	
TW 517359	A	20030111	TW 2001129877	A	20011203	200356	
EP 1356516	A2	20031029	EP 2001272468	A	20011130	200379	
			WO 2001US44952	A	20011130		
AU 2002217986	A1	20020708	AU 2002217986	A	20011130	200427	

Priority Applications (No Type Date): US 2001984259 A 20011029; US 2000742366 A 20001222
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020079562	A1		49	H01L-023/02	CIP of application US 2000742366
WO 200252645	A2	E		H01L-023/498	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZM ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZM ZW

TW 517359	A			H01L-023/28	
EP 1356516	A2	E		H01L-023/498	Based on patent WO 200252645

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR

AU 2002217986	A1			H01L-023/498	Based on patent WO 200252645

Abstract (Basic): US 20020079562 A1
Abstract (Basic):
NOVELTY - An IC die (102) is mounted to the first surface of a substrate (104). **Solder balls** (106) are attached to corresponding exposed contact pads provided to the second surface of the substrate. The first surface of a thermal connector is coupled to the exposed metal plane provided to the second surface of the substrate. The second surface of the thermal connector is configured to be coupled to a printed circuit board.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for an

assembling method of a **BGA** package.
USE - Enhanced die-up **BGA** package.
ADVANTAGE - Provides **BGA** package with improved heat dissipating capabilities, while also providing for high levels of IC electrical performance.
DESCRIPTION OF DRAWING(S) - The figure illustrates a cross-sectional view of a die-up flex **BGA** package with heat spreader.
IC die (102)
Substrate (104)
Solder balls (106)
pp; 49 DwgNo 4/36

6/3,AB/13 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014716814
WPI Acc No: 2002-537518/200257
XRPX Acc No: N02-425630
Ball grid array (**BGA**) packaging that is thermally and electrically enhanced, comprises substrate, stiffener, and several **solder balls** attached to second surface of substrate
Patent Assignee: BROADCOM CORP (BROA-N); KHAN R R (KHAN-I); LAW E (LAWE-I); PAPAGEORGE M (PAPA-I); ZHAO S Z (ZHAO-I)
Inventor: **KHAN R R**; LAW E; PAPAGEORGE M; ZHAO S Z
Number of Countries: 100 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200245164	A2	20020606	WO 2001US44955	A	20011130	200257	B
AU 200217987	A	20020611	AU 200217987	A	20011130	200264	
US 20020135065	A1	20020926	US 2000250950	P	20001201	200265	
			US 2001997272	A	20011130		
EP 1346411	A2	20030924	EP 2001999002	A	20011130	200363	
			WO 2001US44955	A	20011130		

Priority Applications (No Type Date): US 2000250950 P 20001201; US 2001997272 A 20011130
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200245164	A2	E	38	H01L-023/16	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZM ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZM ZW

AU 200217987	A	H01L-023/16	Based on patent WO 200245164	
US 20020135065	A1	H01L-023/48	Provisional application US 2000250950	
EP 1346411	A2 E	H01L-023/16	Based on patent WO 200245164	

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR

Abstract (Basic): WO 200245164 A2
Abstract (Basic):
NOVELTY - **BGA** package (100) includes a substrate (130), stiffener (112), an integrated circuit die (114), a mould/glob top

(120), a number of **solder balls** (122), a first wire connection (124), and a second wire connection (126). The substrate has a base material/dielectric layer (102), a conductive metal layer (106), and a circuit mask (108). The stiffener is attached to the top surface of the substrate by an adhesive (110). The mould/glob is formed over the top surface of the stiffener to encapsulate the die and the first and second wire connections.

USE - In a variety of electronic devices, including telecommunication devices, mobile phones, camcorders, digital cameras, network systems, printers and testers.

ADVANTAGE - The **BGA** packaging is smaller, cheaper, customizable and capable of superior performance when compared with conventional **BGA** packages. The **BGA** package has increased flexibility of die configuration, reduced ball pitch, increased flexibility in circuit routing density, and optional configurations with or without the attachment of a heat sink.

DESCRIPTION OF DRAWING(S) - The drawing is a cross-sectional representation of a **BGA** package design.

BGA package (100)
Dielectric layer (102)
Metal layer (106)
Circuit mask (108)
Adhesive (110)
Die (114)
Mould/glob top (120)
Solder balls (122)
First and second wire connections (124,126)
Substrate (130)
pp; 38 DwgNo 1/18

10/3,AB/1 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

06246203
E.I. No: EIP02527290398
Title: The processing and assembly of liquid crystalline polymer printed circuits
Author: **Zhang, Tan**; Johnson, Wayne; Farrell, Brian; St. Lawrence, Michael
Corporate Source: Auburn University ECE Dept., Auburn, AL 36849-5201, United States
Conference Title: 2002 International Symposium on Microelectronics
Conference Location: Denver, CO, United States Conference Date: 20020904-20020906
E.I. Conference No.: 60397
Source: Proceedings of SPIE - The International Society for Optical Engineering v 4931 2002. p 1-9
Publication Year: 2002
CODEN: PSISDG ISSN: 0277-786X
Language: English
Abstract: Liquid Crystalline Polymers (LCPs) offer a number of advantages in advanced printed wiring board and packaging applications including, low coefficient of thermal expansion, low moisture absorption, low moisture permeability, smooth surface, low dielectric constant and low dissipation at high frequencies, and high temperature capability. This paper examines the processes for manufacturing LCP printed circuit boards, assembly onto LCP boards and fabrication of LCP packages. Specific printed wiring board (PWB) processes examined include lithography and etching, hole formation and metallization, and **solder** mask and surface finish application. The solderability and surface insulation measurements of test coupons passed industry requirements for printed wiring boards. Flip chip assembly and gold thermosonic wire bonding have been demonstrated. Finally, hermetic packages have been fabricated and shown to pass fine and gross leak tests. 9 Refs.

10/3,AB/2 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

08038393 Genuine Article#: 239MM Number of References: 25
Title: AIDS neurologic manifestations in childhood (ABSTRACT AVAILABLE)
Author(s): Rotta NT; Silva C; Ohlweiler L; Lago I; Cabral R; Goncalves F; Almeida AM; **Khan R**; Mello L; Ranzan J; Guedes F
Corporate Source: UNIV FED RIO GRANDE SUL,HOSP CLIN PORTO ALEGRE, SERV PEDIAT, UNIDAD NEUROL INFANTIL/BR-90046900 PORTO ALEGRE/RS/BRAZIL/
Journal: REVISTA DE NEUROLOGIA, 1999, V29, N4 (AUG 16), P319-322
ISSN: 0210-0010 Publication date: 19990816
Publisher: REVISTA DE NEUROLOGIA, C/O CESAR VIGUERA, EDITOR, APDO 94121, 08080 BARCELONA, SPAIN
Language: Spanish Document Type: ARTICLE
Abstract: Introduction. Children with AIDS get infected mainly by vertical transmission. Development. That was what happened in 90% of the cases in a serie of 340 HIV+ children followed at Hospital de Clinicas de Porto Alegre, **Brazil**. Currently, after the use of prophylactic treatment during pregnancy and the six first weeks of life, our transmission rate is 3% to 4%. The incidence of neurologic complications in the vertical transmission group was 49% in our prospective series, and due either to immunosuppression or primary